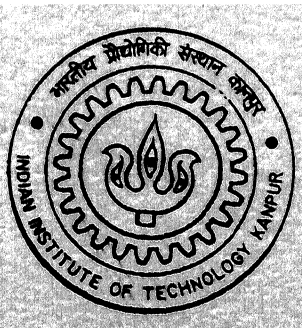
MODELING AND CONTROL OF CONVENTIONAL AND MODIFIED BUCK-BOOST DC-DC CONVERTER

by

RAVINDRA KUMAR SINGH



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

JUNE 2001

MODELING AND CONTROL OF CONVENTIONAL AN MODIFIED BUCK-BOOST DC-DC CONVERTER

A Thesis Submitted
in Partial Fulfilment of the Requirements
for the degree of

DOCTOR OF PHILOSOPHY

by

RAVINDRA KUMAR SINGH

to the

DEPARMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY KANPUR
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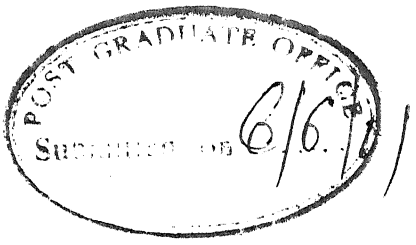

CERTIFICATE

This is to certify that the work contained in the thesis entitled "**Modeling and Control of Conventional and Modified Buck-Boost DC-DC Converter**" by Ravindra Kumar Singh has been carried out under our supervision and this work has not been submitted elsewhere for a degree.

Avinash Joshi

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Department of Electrical Engineering
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Avinash Joshi

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Department of Electrical Engineering
Indian Institute of Technology
Kanpur, India

Dedicated To

the memory of

my beloved mother

Smt. Shanti Devi

ACKNOWLEDGEMENTS

With the deepest sense of gratitude I express my indebtedness to my supervisors Prof. Avinash Joshi and Prof. Arindam Ghosh for their active participation, constant guidance, best supervision and moral support during this dissertation work.

I am thankful to my teachers Prof. G. K. Dubey, Prof. Sachchidanand, Dr. B. G. Fernandes including my supervisors for their motivation and support.

My regards are due to Prof. L. P. Singh for his constant encouragement and motivation.

I will like to thank intimate friends namely Ajai Garg, Jayaram sir, Bisdas, Mahapatra jee, Kishor dada, Jamal, Gopi Natha, Ramesh, Mahesh, K. K. Singh, Subrato Ghosh, Subhash Mishra, Manoranjan Sinha, Mudgil, Alok Srivastava, Lt. Sachdeva, Hemant, Mr. R. P. Gupta, Mr. P. V. K. Reddy jee for active interaction on every topic. My special thanks are to Mr. Gopesh Tiwari for helping me in the best possible way in my last phase of the program.

My thanks are due to Mr. Alok Gupta, Manish Agarwal, Santanu Metia who helped me testing and fabrication of hardware.

I wish to thank Mr. Imran Khan of winding shop, Mr. Tiwari of electrical workshop, Mr. Manoj of electrical stores and many others for helping me during fabrication work.

I am thankful to my esteemed colleagues at my parent institute Moti Lal Nehru Regional Engineering College, Allahabad for their encouragement and sharing of academic load during this program.

I am indebted to my father and parent in law who stood by me during the most difficult times through out this project.

I thank my wife Poonam for her mental support and forbearance throughout my thesis work. I thank my daughter Swarnima and my son Aditya who keep my spirit alive.

Finally I thank all of persons who have helped me directly or indirectly in the process of completion of the work.

Ravindra kumar Singh

June 2001

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Degree for which submitted:	**Ph. D.**

SYNOPSIS

A good regulated DC power supply is needed for general purpose electronic products like microwave ovens, laser printers, medical instruments, stereos, televisions, electronic lighting, personal computers to sophisticated equipment to be used in aerospace applications or satellite control equipment. A regulated power supply should be able to produce a constant output voltage without loosing stability against load and supply voltage changes [1]. It is also desired that the regulated power supply is capable of tracking a change in reference command. Besides these, there are other considerations for a DC power supply. Miniaturization of the power supply is a growing requirement for space saving and cost effectiveness of utilities. Electromagnetic Interference (EMI) compatibility, loss minimization, etc. are some of the other factors.

A regulated power supply must be able to cater to widely varying loads and power supply conditions. This requires a closed loop control design of the converter that gives a stable operation for maximum possible loads conditions and supply disturbances at a reasonable high-speed. To design a closed loop controller for the converter and to study the stability of closed loop system, a mathematical model which describes the dynamics of the open loop system is required. The DC-DC converter is a switched piece-wise linear circuit. Its input is duty ratio and output is the output voltage. In the solution of piecewise linear model, the duty ratio appears in exponential form. Therefore the input-

output relation is nonlinear and not suitable for closed loop control design. Hence a suitable model must be obtained that can be used for control design.

A model for the converter must be able to address following issues:

- The equations describing the dynamics should be consistent with the actual behavior.
- The mathematical equation must be in closed form that is suitable for closed-loop controller design.
- The model must be able to describe the converter operation for all possible operating points.

A number of models of converters operating in closed loop and open loop are proposed in literature. These models either converges to State Space Average (SSA) model proposed by Middlebrook [2] or can be derived from the SSA. The SSA models, though simple, but have limited validity for perturbation around an operating point. This restricts the controller operation limits, i.e. the controller works only for a very small zone around the operating point. To handle larger perturbations, a better model is required. An improvement in model prediction was reported in [3]. The average output voltage equation has been derived without averaging any circuit states and thus has a better performance than SSA. Using this linear model, a controller can handle larger perturbation compared to controller designed on the basis of the SSA model of the converter. It is however desirable to increase the perturbation zone even further from the point of view of robustness of operation.

A closed loop controller has its parameters designed for a given parameter set of the system. If the system parameters are valid for a wider range, then the closed loop system will have large area of operation. The modeling error therefore must be as small as possible over a wide range. This requires a new model suitable for better control design.

The closed loop system may have a number of performance indexes for achieving desired dynamic response, but the stability is of paramount importance. Normally, the

nonlinear systems are linearized using Taylor's series expansion. The linear model thus derived has a limited validity. To widen the validity zone, affine terms of Taylor's series expansion are taken in model. This makes the system nonlinear. Therefore nonlinear controller design techniques are applied to guaranty stability. The design philosophy of these systems can be based on Lyapunov's method [4].

The fast dynamic response is another important criterion for a regulated power supply. A number of research works are reported in literature for improving the speed of the closed loop response. There are two ways to improve the dynamic response - first by designing a better closed loop control strategy as in [5] or by improving the topology itself [6].

In the view of the above discussions, the objectives of the thesis are as follows:

- To derive a perturbation model of a given DC-DC converter, which has larger validity zone compared to the existing models.
- To design a closed loop controller for the proposed converter using model derived.
- To explore the possibility of finding a new converter topology that can improve the dynamic response.
- To design a closed loop controller for the proposed new converter topology.

To achieve the above mentioned objective research work is carried out in this thesis. The major contributions of the thesis are

(1) A new discrete time model has been derived. It has been given the name of Bilinear Corner Point (BCP) prediction model. Let the end point refers to a point in time at which the switch is closed. The model is derived by expanding the equation of an end point in terms of the previous end point and duty ratio by Taylor's series. The bilinear term are retained while the second and higher order terms are neglected as the bilinear term's contribution is more significant. Based on the BCP model, a model for obtaining average of the voltage and the current is also proposed. A

generalized converter model has been derived. This model has been called generalized as it is shown that the linear corner point model [3], the BCP prediction model and SSA models can be derived from the proposed model. All the models proposed have been verified by extensive simulation and experiments on a Buck-Boost converter. The same modeling approach can however be extended to other DC-DC converters.

(2) Closed loop operation of converter based on the bilinear model has been done and verified by extensive simulation and experimentation. The controller is designed based on feedback linearization using Lyapunov's direct method. A supplementary linear controller is also used. The linear controller can be designed using either pole placement technique or minimizing a linear quadratic performance index.

(3) A multi-zonal fuzzy controller based on bilinear model of the converter has been derived. The fuzzy controller has been verified by simulation studies. The fuzzy based controller has a larger zone of closed loop operation compared to feedback linearized controller.

(4) A new topology called modified buck-boost converter [7] has been proposed. This converter allows simultaneous opening of inductor charging switch and load capacitor charging switch. To do so, an energy recovery winding with an uncontrolled diode or a switch is required. The steady state characterization of converter has been done at constant frequency operation by circuit averaging theorem and has been verified experimentally. The converter can be operated in buck or boost modes depending on the duty ratio of main and load switches. A small signal perturbation model of the converter has been developed.

(5) A variable frequency closed loop control strategy for the modified buck-boost converter has been proposed. In this scheme, the inductor current and the output voltage are forced to operate within a pre-decided hysteresis band. The load and supply changes are rejected at the cost of the energy recovery interval. The closed loop controller takes in account of cold starting and overload conditions.

(6) The proposed two switch modified buck-boost converter has been extended for multiple outputs. The steady state characterization of multiple output converters at variable frequency has been done. The closed loop operation of converter using hysteresis controller at variable frequency has been performed. The feasibility and operation are established through simulation and experimentation.

OUTLINE OF THE THESIS

Chapter 1 introduces the objective of the thesis and outlines briefly the work done in the thesis. A brief literature review of modeling, controller design for hard-switched PWM converters has been included. The chapter also outlines other issues of DC-DC converter like fast response and multiple output control and design issues reported in literature.

In Chapter 2, mathematical modeling of the buck-boost converter has been reported. Two models are derived called bilinear corner point prediction model and average model. Furthermore a generalized model has also been derived and it has been shown that many models are subsets of the generalized model. Extensive simulation studies are performed to validate the models derived along with some experimental results.

In Chapter 3, the closed loop controller has been designed for buck-boost converter using the BCP prediction model. A pseudo-integrator has been used to facilitate reference tracking. Simulation and experimental results with both linear and bilinear models are presented. Further a multi-zonal fuzzy controller is designed that has a very wide range of operation. This controller is validated through extensive simulation studies.

In Chapter 4 an alternate converter topology called modified flyback converter is proposed. The steady state operation of the converter at constant frequency has been analyzed. The single output converter topology is extended for multiple output. The steady state operation of converter and its characterization has been done. A small signal perturbation model of the single output converter has also been derived. The steady state characteristics have been validated by extensive simulation study and experimentation.

In Chapter 5, a closed loop hysteresis controller for modified buck-boost converter is proposed. The proposed controller has been validated by simulation studies and experimentation. The same controller concept has been extended for multiple output converters. The simulation and experimental results are given for validation of closed loop operation of multiple-output converter.

In Chapter 6, the details of experimental setups used for thesis work have been given. Details of the power circuits, various control circuits are presented. The real time control computations for buck-boost converter are done in an IBM compatible personal computer (PC). The PC interface circuit has also been discussed in the chapter. The hardware design and algorithms used for realization of controllers are described in detail.

The thesis concludes in Chapter 7, which outlines major contributions and also suggests scope of future work in this area.

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LIST OF SYMBOLS

T	Switching Frequency of Converter
t	Instantaneous time
t_{onM}	Time interval for which main switch of two-output modified converter is ON.
t_{on1}	Time interval for which load switch 1 of two-output modified converter is ON.
t_{on2}	Time interval for which load switch 2 of two-output modified converter is ON.
f	Frequency of operation of Converter
d	Duty Ratio
d_0	Steady state duty ratio
$\tilde{d}$	Perturbation in duty ratio
Sw	An ideal controlled Switch normally realized in practice by MOSFET, IGBT
D	Fast Recovery Diode and Duty ratio of the main switch in modified converter in Chapter 4
V_{dc}	Supply Voltage of a dc-dc converter
ΔV_{dc}	Change in supply Voltage of a dc-dc converter
R	Load Resistance for single output converters
ΔR	Perturbation in load resistance for single output converters
R_1	Load Resistance on Output 1 of Two-output converters
R_2	Load Resistance on Output 2 of Two-output converters
R_c	Critical resistance for modified converter

R_L Winding resistance of inductor having inductance of L.

L Inductance of buck-boost converter

L_1 Inductance of main inductor winding of modified converter

L_2 Inductance of energy Recovery inductor winding of modified converter

C Capacitor of Buck-Boost Converter

esr Series resistance of capacitor

C_1 Capacitance at the output 1 of Two-Output converter

C_2 Capacitance at the output 2 of Two-Output converter

V_0 Output Voltage of a converter of single output converters

$V_{0,ref}$ Reference output voltage of a converter of single output converters for hysteresis controller

V_{01} Output Voltage 1 of a converter of two-output converters

V_{02} Output Voltage 2 of a converter of two-output converters

x State variable used in state space analysis

$\tilde{x}(.)$ Perturbation in state vector

x_{av} Average or dc value of the state vector x

$\tilde{x}_{av}$ Perturbation in x_{av}

v_C Voltage across Capacitor in a converter circuit

i_L Inductor Current

A_i, B_i, C i^{th} State and input matrix and output matrix

Φ Sate Transition matrix

Θ Convolution Matrix of state transition matrix with input matrix and forcing input

x_0 Steady state vector

$x(t_i)$ Magnitude of sate vector at instant t_i

CP **C**orner **P**oint

BCP **B**ilinear **C**orner point **P**rediction

k Discrete index of time instant

SSP Simulated System Perturbation

LMP Linear Model Prediction

BMP Bilinear Model Prediction

SSA State Space Averaging

$\tilde{y}_{ref}$ Change in the reference voltage

$e(k)$ Error

$z(k)$ Integral state variable

$\tilde{x}_e(k)$ Perturbation of extended state vector

$\tilde{u}(k)$ Perturbation in the input or duty ratio same as $\tilde{d}(k)$

λ Pole shift factor

J linear quadratic performance index

$\Re$ Positive scalar penalty on the control

$V(k)$ Lyapunov function candidate

K_i Gain of integral block of a closed loop controller

A_i i^{th} Fuzzy set

w_i Value of the i^{th} membership function

x_{0w} Fuzzy estimate of the initial condition

N_1 Number of turns in the winding of inductance L_1 of two-Output Converter

N_2 Number of turns in the winding of inductance L_2 of two-Output Converter

$a = N_1 / N_2$ Turn Ratio

Sw_m Main switch of the modified converter

Sw_1, Sw_2 Load switches

D_{sw} Diode in series with load switch of modified converters

$\Im$ Core mmf

$\Im_{av}$ Average Core mmf

$\Im_{max}$ Maximum value of the core mmf in hysteresis controller

$\Im_{min}$ Minimum value of the core mmf in hysteresis controller

d_{ER} Energy recovery ratio or duty

d Load duty ratio for single output modified converter

d_1 Duty ratio of load switch 1 of two outputs modified converter

d_2 Duty ratio of load switch 2 of two outputs modified converter

CHAPTER 1

INTRODUCTION

A good regulated DC power supply is needed for general purpose electronic products like microwave ovens, laser printers, medical instruments, stereos, televisions, electronic lighting, personal computers to sophisticated equipment that are used in aerospace applications or satellite control equipment. A regulated power supply should be able to produce a constant output voltage without losing stability against load and supply voltage changes [1-6]. It is also desired that the regulated power supply be capable of tracking a change in reference command. Besides these, there are other considerations for a DC power supply. Miniaturization of the power supply is a growing requirement for space saving and cost effectiveness of utilities. Electromagnetic Interference (EMI) compatibility, loss minimization, etc. are some of the other factors.

1.1 CLASSIFICATION OF DC-DC CONVERTERS

There are two types of regulated DC power supply- linear power supply and switched mode power supply. The linear power supply operates as an active resistance controlled circuit. The ac power is rectified at power frequency by uncontrolled diode rectifier and then filtered to produce a smooth dc voltage. This filtered DC voltage is then fed to a series active element. The series element acts a variable controlled resistor, which is placed in the series with load. The series resistance is made small as load increases and the resistance is made

large at light loads. Thus, the power supply regulates the output voltage constant for all loading conditions. The control is exercised by feedback of the output voltage by a controller, which regulates the variable series active resistance. Since the output current passes through the controlled series resistance, there is very large heating loss in the linear power supply. The cooling requirement for linear power supply is thus very high and it requires large size heat sinks. The heating therefore not only reduces the efficiency of conversion but also make it more bulky. Thus, linear power supply is just a matter of historical importance. The drawbacks listed resulted in the growing population of switch mode power supply.

In switch mode regulated power supply, ac power is rectified to get a dc power and this dc power is chopped to regulate the output voltage by turning ON and OFF controlled silicon switches. The switch when ON ideally has zero voltage across the device and hence no power loss. When OFF, it has zero current flowing through and hence power loss is zero. Ideally switch mode power supply works with zero power loss across the switching element. It has therefore higher efficiency. The output voltage of the converter is regulated by control of ON-OFF periods of the silicon switch. The voltage grading and isolation is provided by high frequency transformer connected to high frequency ac obtained from line rectified dc source. Due to high frequency, the size of the transformer and hence of the converter is reduced substantially.

Although there are numerous switch mode converter circuits described by a number of authors, basically all of them are related to three classical circuits known as the "flyback or buck-boost converter," the "forward or buck," and the "push-pull or buck-derived" converter. The circuit diagram of buck-boost converter is shown in Fig. 1.1 as an example. When the switch Sw is closed, current flows through inductor L, storing energy. Because of voltage polarity, diode D is reverse biased, thus no voltage is present across the load R unless the capacitor is charged. In that case the capacitor keeps discharging due to the load resistance. When the switch is opened, the voltage across inductor L reverses polarity because of collapsing magnetic field, forward biasing diode D, and inducing a current flow though the load and capacitor. This builds a voltage V_0 across the capacitor with the polarity as shown.

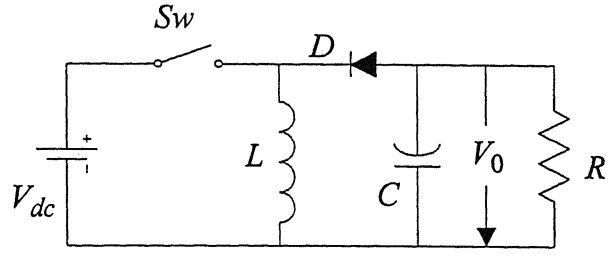


Fig. 1.1 Buck-Boost Converter

It is to be noted that the switch Sw is opened when it is carrying full current and closed at full supply voltage V_{dc}. Due to non-ideal nature of the switch, there are substantial switching losses in these devices at the time of turning ON and OFF. This has attracted a number of researchers to go for an alternate topology that can reduce switching losses [7-14]. This essentially require designing a circuit in which the controlled switch turns ON and OFF at zero voltage or zero current, thereby making the switching loss to go to zero. A number of such circuits are proposed in literature, which can be grouped together and can be called soft switched converters. They are named soft switched to demarcate them from classical switch mode converter circuits where switching is done at full voltage and current. This switching is now commonly referred to as hard-switched PWM converters.

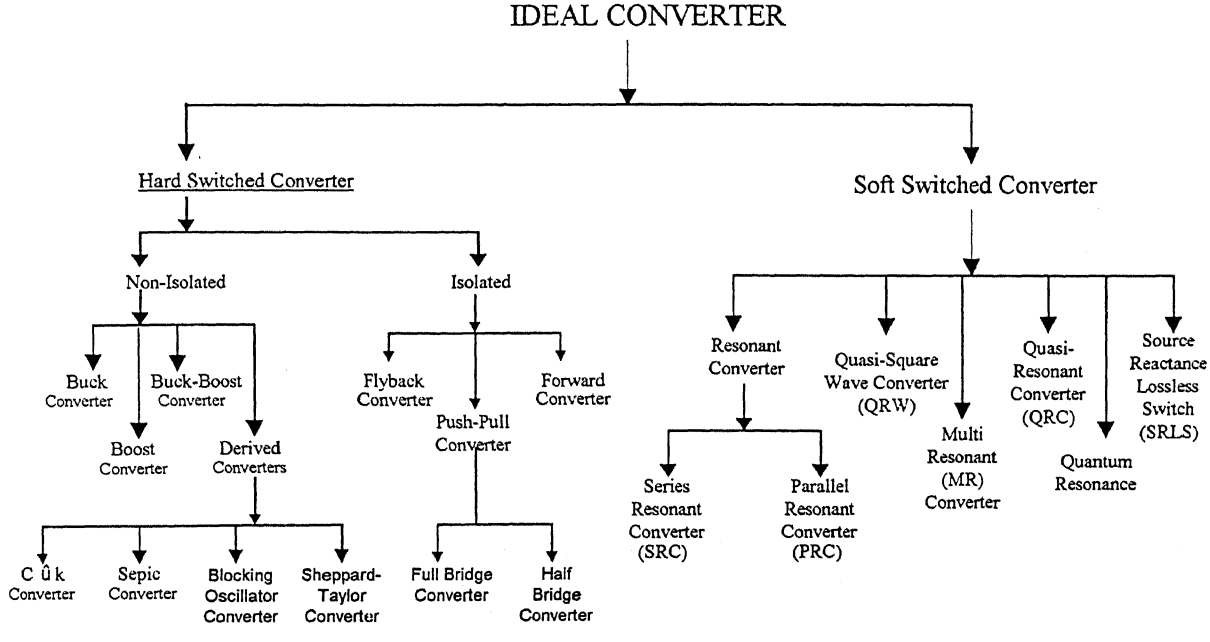


Fig. 1.2 Classification of the DC-DC converters

All soft switch converter topologies proposed in literature have first and prime focus on zero voltage (ZVS) or zero current switching (ZCS), whereas the hard switched converters are mainly meant for getting desired conversion ratio and isolation between input and output. A classification of the DC/DC converters is shown in Fig. 1.2. A standard buck-boost converter has been taken for verifying theories proposed in the thesis. However, the principals derived for buck-boost converter can easily be extended to all hard-switched converters in general.

1.2 MODELING OF DC-DC CONVERTER

A regulated power supply must be able to cater to widely varying loads and power supply conditions. This requires a closed loop control design of the converter that gives a stable operation for maximum possible loads conditions and supply disturbances at a reasonable high-speed. To design a closed loop controller for the converter and to study the stability of closed loop system, a mathematical model which describes the dynamics of the open loop system is required. The DC-DC converter is a switched piece-wise linear circuit. Its input is duty ratio and output is the output voltage. In the solution of piecewise linear model, the duty ratio appears in exponential form. Therefore the input-output relation is nonlinear and not suitable for closed loop control design. Hence a suitable model must be obtained that can be used for control design.

A model for the converter must be able to address the following issues:

- The equations describing the dynamics should be consistent with the actual behavior.
- The mathematical equation must be in closed form that is suitable for closed-loop controller design.
- The model must be able to describe the converter operation for all possible operating points.

The system to be modeled can be represented in time domain as well as in the frequency domain. The closed loop controller can be designed in time domain and frequency domain. Therefore, the literature is full of models in both time domain [15-33] and frequency

domain [34-36]. The state space (SSA) model proposed by Middlebrook [15] is most popular because of its simplicity. The modeling is done in continuous time. The converter switching at discrete instants makes discrete – time modeling of the converter a natural choice [17,18,23,37]. Various converter-modeling approaches are listed in Fig. 1.3.

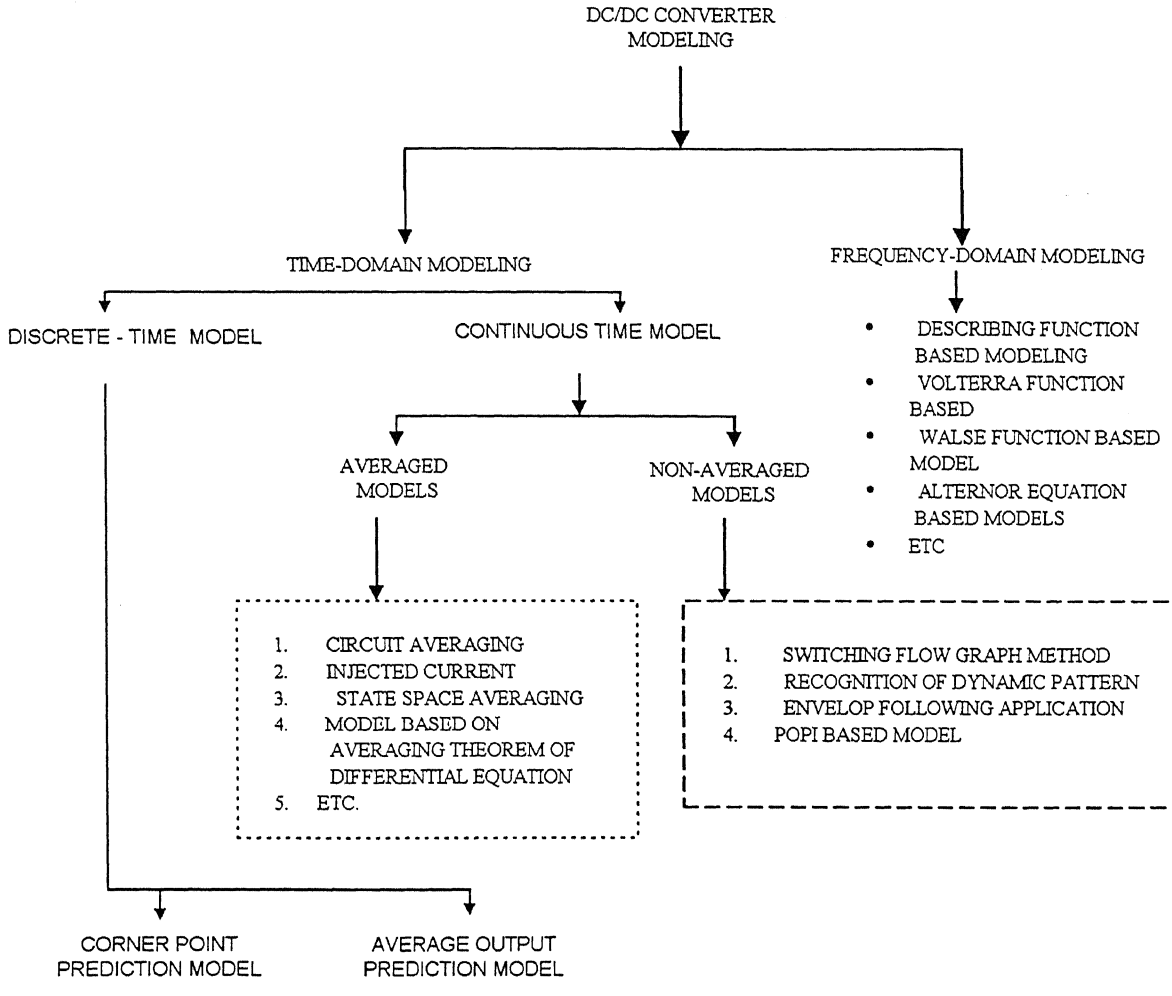


Fig. 1.3 Various modeling approaches of DC-DC converter

We shall briefly review some of the modeling techniques and their limitations. One of the classical modeling methods is known as the averaging technique. The averaging technique assumes low ripple in voltage and current and hence these quantities are assumed to be constant over a cycle. An averaged equivalent circuit of the converter is obtained by averaging the states and other variables of the converter over a cycle. The parameters under consideration are then perturbed and simplified to obtain perturbation model of the converter.

This method has been extended for SSA modeling. The small ripple approximation requires very high frequency of operation and hence it fails for an actual converter where the ripple contents can not be assumed to be zero. Further, this method is valid only for continuos conduction mode (CCM) operation, as small ripple in all of the variable of a converter is possible with CCM operation. Injected current method provide another closed loop model, which takes in account of both continuos and discontinuous conduction mode of operations of the converter. In this method, the mathematical equation are written for output voltage in terms of segment of inductor current injected to output circuit and small signal approximation is then applied to this equation to obtain the small signal perturbation model. Again to reiterate, the application of small ripple approximation results in large errors.

The state space averaging [15,16] is the most widely used DC-DC converter model. This model is derived for converters operating at high frequency hence have low ripple content in current and output voltage. The average state space equation is time average sum of state equations for the respective intervals. The detail of the method has been given in Chapter-2.

A number of nonlinear techniques in time domain and frequency domain have been used in modeling of DC-DC converters. Windowed Fourier transform technique and KBM (Krylov – Bogoliubov - Mitropolsky) approximation method or classical averaging theory are the ones used extensively in literature for modeling in time domain. To apply averaging theorem, the differential equation representing the dynamics of the converter must be written in standard form as given by:

$$\dot{x} = \varepsilon\, f(x,t); \quad where\ \varepsilon << 1, \&\ x(t_0) = x_0 \tag{1.1}$$

and $f(x,t)$ should be analytic function of x and t. By averaging theorem, (1.1) can be simplified to,

$$\dot{y} = \varepsilon\, G(y); \quad y(t_0) = y_0 \tag{1.2}$$

where

$$G(y) \overset{\Delta}{=} \lim_{T\to\infty} \frac{1}{T} \int_0^T f(s,y)ds \tag{1.3}$$

The representation of the dynamic equation in (1.1) requires a very small quantity ε,

which is normally taken as the switching period of the converter i.e. $\varepsilon = T$. This implies that the converter operates at high frequency given in [21,22]. Further simplification of the windowed Fourier transform has been used in literature. The converter dynamic equation is expressed in terms of constituent dynamics of the harmonic components [19]. This method approximates the average dynamics by average component of the Fourier series and ripple dynamics by other harmonics. The average dynamics turns out to be the same as to that of the SSA model.

Besides these, a number of models are reported in literature to account for the other circuit considerations such as accounting for parasitic elements of the converter [29], discontinuous conduction mode (DCM) operation of the converter [24,27], etc. Closed loops modeling of the converters are also reported in the literature [16,25,28,30,32,39]. These models can be easily derived from the concept leading to the development of SSA.

A natural choice for DC-DC converter simulation is the time domain simulation [40-42]. However frequency domain has also been reported [43]. These models are based on various principle like use of alternor equation [40], MISSCO concept [44], POPI concept [45], etc. But these models can not be used for closed loop controller design.

A discrete time average model has been proposed in [37]. This model does not average the states as done in SSA. The average value has been computed by direct integration of the solution of the dynamic equation of the converter over a cycle. The average value is then given a perturbation to obtain the perturbation model. This model predicts better than the SSA model for large ripples at lower frequency. However, the model is valid only over a small range of perturbation in duty ratio. In the thesis this model has been extended to take in account of larger perturbation in the duty ratio. This has been achieved by considering higher order terms in the expansion of the perturbation model. The model given in [37] takes in account for a converter working with two intervals in a switching cycle. This has been extended in present thesis work to consider multi interval system.

1.3 CONTROL OF DC-DC CONVERTERS

The converter is to be operated in closed loop to reduce the sensitivity of the noise and parameter variations of the converter system. The design of the controller is a strong function of the model of the system to be controlled and various performance indices specified to meet the closed loop requirements. But the stability of a system is of paramount importance [46].

The challenges of the closed loop control design are to account for modeling inaccuracy, measurement disturbance, parameter variations and other aspects. Various techniques of control design have been reported in literature [46-53]. Most of these controllers have been designed for converter modeled by SSA. The SSA model is represented by linear or bilinear differential equation. Therefore the controller design for continuous time system has been extended in these controllers. The bilinear SSA model is although nonlinear but continuos. A number of works has been reported to design a closed loop controller for the converter represented by bilinear model [51-53]. Since the bilinear model is nonlinear model, all these controllers are based on Lyapunov's stability theorem.

If the modeling error is reduced, the controller will work for a larger zone. But, is it possible to increase the zone of validity further by modifying or changing the controller? The answer to this question is yes as a change in the control strategy can bring an increase the zone of operation. There are number of linear and nonlinear control methods reported in literature and books like pole placement method or linear quadratic regulator method or variable structure control method or fuzzy control. Its is a matter of specifying the objectives for the closed loop system for choosing a control technique. If a linear feedback control law is used in the closed loop, Lyapunov's theorem has to be applied to ensure stability, since the converter model is nonlinear. But how the amalgamation of the two, i.e. linear control law and Lyapunov's theorem is to be done is a matter of design.

The requirement of tracking requires an integral controller in control loop. The system is represented by the bilinear model. The closed loop controllers are derived by using Lyapunov's stability theorem [51-53]. The integral controller places a pole at the origin and which makes difficult to obtain P matrix of the Lyapunov function. In this thesis, two methods are suggested to address this problem and called Pseudo-integral and pure integral based

controllers.

1.4 MODIFICATION OF TOPOLOGY FOR FASTER RESPONSE

The end goal of the closed loop converter system is to improve dynamic response and regulation against supply and load change. This can be accompanied by a change in closed loop control strategy as reported in [54] or a change in topology as reported in [55,56]. The change in topology for hard-switched converter has also been done for improvement in cross regulation of a multiple output converters [57-60].

Let us take an example of classical buck-boost converter. The circuit diagram of the converter is shown in Fig. 1.1. It has a controlled switch in the input side which allows the inductor current to be turned ON and OFF at the desired levels. But, the diode in the output circuit forces the output capacitor to be charged for the entire OFF period of the controlled switch. The regulation of the capacitor voltage is possible only by changing the OFF period of the switch, which is complement of the ON period if the converter is operating in the CCM at constant frequency. Therefore the control of the output voltage is not direct.

There are primarily three types of disturbances possible in any converter. These are input or source deviation from its nominal value, load fluctuation from its rated value and parameter alteration. These may be due to various possible reasons, such as poor ac source regulation, rapidly changing loads, saturation of magnetic core, etc. The input supply variations can be retracted optimally in time [54], often in one cycle by controlling the switch of the conventional converter. To take in account of parameter variation along with other control objectives, adaptive or robust controller has been extensively used in literature [47,50]. The dynamic response is seldom taken as closed loop parameter in controller design and therefore the system dynamic response is normally poor. Even if the time optimization of the response is done, the natural circuit time constant cannot be reduced and hence faster operation beyond a certain limit is not feasible.

The natural circuit time constant is a function of inductance, capacitance and load resistance of the converter. The parameter values are chosen such that the converter's steady state performance criteria are met. The choice of parameter values do not take in account of

performance indices of closed loop controller Therefore the dynamic response of conventional buck-boost converter does not improve beyond a limit due to topological limitations. Therefore, a topology is required for rejection of the various disturbances in optimal time.

A multiple output DC-DC converter consists of a supply and a number of regulated outputs [57]. The power circuit of such converters may use either flyback or forward topology. The control design of such converters is aimed at providing constant and stable output voltages at individual outputs for admissible load and input voltage changes. Regulation against load changes of individual outputs by different methods reported in literature has a minimum error in all outputs. In [59] the circuit topology has been modified to minimize the errors in outputs by magnetic coupling of secondary windings. In [58] one output is operated in Continuous Conduction Mode (CCM) and the other output in Discontinuous Conduction Mode (DCM) to regulate load perturbations in a dual converter. However the uncontrolled charging of the capacitors do not allow independent regulation of the outputs and the response time is a strong function of the system parameters and the switching frequency. This therefore requires a modification in the basic topology.

1.5 OBJECTIVES AND CONTRIBUTIONS OF THE THESIS

In the view of the above discussions, the objectives of the thesis are as follows:

- To derive a perturbation model of a given DC-DC converter, which has larger validity zone compared to the existing models.
- To design a closed loop controller for the proposed converter-using model derived.
- To explore the possibility of finding a new converter topology that can improve the dynamic response.
- To design a closed loop controller for the proposed new converter topology.

To achieve the above mentioned objective research work is carried out in this thesis. The major contributions of the thesis are

(1) A new discrete time model has been derived. It has been given the name of Bilinear

Corner Point (BCP) prediction model. Let the end point refer to a point in time at which the switch is closed. The model is derived by expanding the equation of an end point in terms of the previous end point and duty ratio by Taylor's series. The bilinear term are retained while the second and higher order terms are neglected as the bilinear term's contribution is more significant. Based on the BCP model, a model for obtaining average of the voltage and the current is also proposed. A generalized converter model has been derived. This model has been called generalized as it is shown that the linear corner point model [3], the BCP prediction model and SSA models can be derived from the proposed model. All the models proposed have been verified by extensive simulation and experiments on a Buck-Boost converter. The same modeling approach can however be extended to other DC-DC converters.

(2) Closed loop operation of converter based on the bilinear model has been done and verified by extensive simulation and experimentation. The controller is designed based on feedback linearization using Lyapunov's direct method. A supplementary linear controller is also used. The linear controller can be designed using either pole placement technique or minimizing a linear quadratic performance index.

(3) A multi-zonal fuzzy controller based on bilinear model of the converter has been derived. The fuzzy controller has been verified by simulation studies. The fuzzy based controller has a larger zone of closed loop operation compared to feedback linearized controller.

(4) A new topology called modified buck-boost converter [56] has been proposed. This converter allows simultaneous opening of inductor charging switch and load capacitor charging switch. To do so, an energy recovery winding with an uncontrolled diode or a switch is required. The steady state characterization of converter has been done at constant frequency operation by circuit averaging theorem and has been verified experimentally. The converter can be operated in buck or boost modes depending on the duty ratio of main and load switches. A small signal perturbation model of the converter has been developed.

(5) A variable frequency closed loop control strategy for the modified buck-boost converter has been proposed. In this scheme, the inductor current and the output voltage are forced to operate within a pre-decided hysteresis band. The load and supply changes are rejected at the cost of the energy recovery interval. The closed loop controller takes in account of cold starting and overload conditions.

The proposed two switch modified buck-boost converter has been extended for multiple outputs. The steady state characterization of multiple output converters at variable frequency has been done. The closed loop operation of converter using hysteresis controller at variable frequency has been performed. The feasibility and operation are established through simulation and experimentation.

1.6 LAYOUT OF THE THESIS

Chapter 1 introduces the objective of the thesis and outlines briefly the work done in the thesis. A brief literature review of modeling, controller design for hard-switched PWM converters has been included. The chapter also outlines other issues of DC-DC converter like fast response and multiple output control and design issues reported in literature.

In Chapter 2, mathematical modeling of the buck-boost converter has been reported. Two models are derived called bilinear corner point prediction model and average model. Furthermore a generalized model has also been derived and it has been shown that many models are subsets of the generalized model. Extensive simulation studies are performed to validate the models derived along with some experimental results.

In Chapter 3, the closed loop controller has been designed for buck-boost converter using the BCP prediction model. A pseudo-integrator has been used to facilitate reference tracking. Simulation and experimental results with both linear and bilinear models are presented. Further a multi-zonal fuzzy controller is designed that has a very wide range of operation. This controller is validated through extensive simulation studies.

In Chapter 4 an alternate converter topology called modified flyback converter is proposed. The steady state operation of the converter at constant frequency has been analyzed.

The single output converter topology is extended for multiple output. The steady state operation of converter and its characterization has been done. A small signal perturbation model of the single output converter has also been derived. The steady state characteristics have been validated by extensive simulation study and experimentation.

In Chapter 5, a closed loop hysteresis controller for modified buck-boost converter is proposed. The proposed controller has been validated by simulation studies and experimentation. The same controller concept has been extended for multiple output converters. The simulation and experimental results are given for validation of closed loop operation of multiple-output converter.

In Chapter 6, the details of experimental setups used for thesis work have been given. Details of the power circuits, various control circuits are presented. The real time control computations for buck-boost converter are done in an IBM compatible personal computer (PC). The PC interface circuit has also been discussed in the chapter. The hardware design and algorithms used for realization of controllers are described in detail.

The thesis concludes in Chapter 7, which outlines major contributions and also suggests scope of future work in this area.

CHAPTER 2

MODELING OF DC-DC CONVERTERS

A dc-dc converter is a switched dc circuit, which due to its periodic switching has nonlinear behavior even when all its circuit elements are linear. The control variable is the duty ratio and there is no linear relationship between the duty ratio and the output voltage. Therefore, one approach of modeling such a circuit is to determine a suitable linear models applicable around a dc operating point.

In this chapter, we shall derive two perturbation models – one of which is linear and the other is bilinear. Both these models are derived from Taylor's Series expansion of the state transition equations governing the operation of the dc-dc converters. We shall compare these models with commonly used State Space Averaging (SSA) technique. Finally a generalized derivation for finding the perturbation model will be presented.

2.1 STATE TRANSITION EQUATIONS OF DC-DC CONVERTER

A hard-switched PWM dc-dc converter has at least a controlled switch, a diode and an inductor connected in some way to operate in buck, boost or Buck-Boost mode. The converter can be switched at a constant frequency or variable frequency. For a constant frequency operation, the circuit is switched periodically with a time period of T. The switch remains closed for dT, and open for $(1-d)T$ in each cycle, where $d\,(0 \le d \le 1)$ is called the

duty ratio of switching. The timing diagram for this switching is shown in Fig. 2.1. For steady state operation, points like t_0 & t_2 where the switch is closed are termed as the corner point (CP). This is indicated in Fig. 2.1.

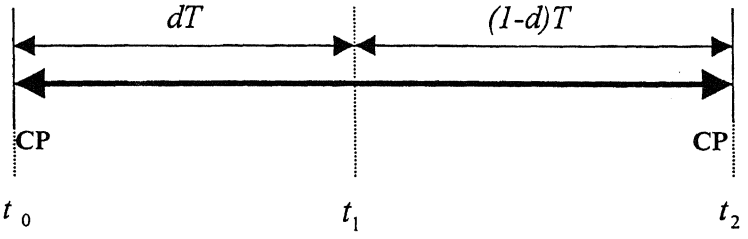


Fig. 2.1 Switching time diagram for converters operating at constant frequency.

It is interesting to note that the circuit topology and hence the dynamic equations governing the converter circuit change in two the periods mentioned above. However, the state variables such as currents through inductors and voltages across capacitors remain continuous.

For example, consider a Buck-Boost converter circuit shown in Fig. 1.1 repeated below as Fig. 2.2. In this circuit, it is assumed that the converter operates in Continuous Conduction Mode (CCM) at constant frequency and the switch *Sw*, the inductor (*L*) and capacitor (*C*) are ideal. The equivalent circuit with switch *Sw* closed and open are shown in Fig. 2.3 and Fig. 2.4 respectively. The switch in ON condition reverse biases the diode due to supply voltage. This turns OFF the diode. When the switch is OFF, the inductor current forces a forward current through the diode and diode starts conducting.

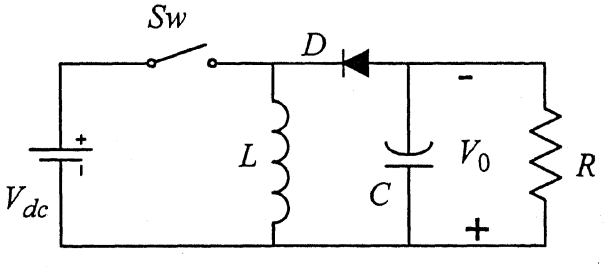


Fig. 2.2 *Buck-Boost Converter*

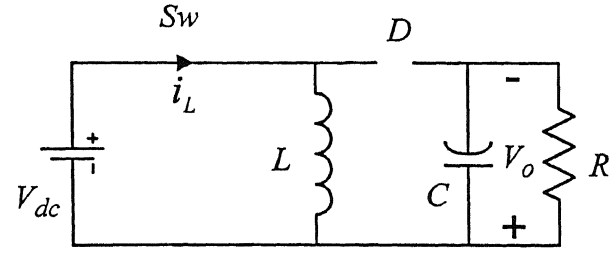


Fig. 2.3 Equivalent circuits when the switch is ON

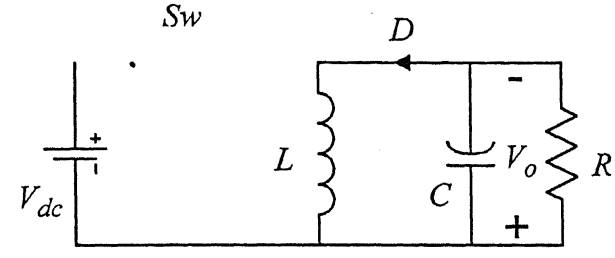


Fig. 2.4 Equivalent circuits when the switch is OFF

Defining a state vector $x^T = [v_C \quad i_L]$, we get the following state space description when the switch is closed, i.e. from Fig. 2.3

$$\frac{dx}{dt} = \begin{bmatrix} -1/RC & 0 \\ 0 & 0 \end{bmatrix} x + \begin{bmatrix} 0 \\ 1/L \end{bmatrix} V_{dc} = A_1 x + B_1 V_{dc} \tag{2.1}$$

and the state space equation for the switch open (Fig. 2.4) is given by

$$\frac{dx}{dt} = \begin{bmatrix} -1/RC & 1/C \\ 1/L & 0 \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{dc} = A_2 x + B_2 V_{dc} . \tag{2.2}$$

The output equation in either case is the capacitor voltage and hence is given by

$$v_o = [1 \quad 0] x = C_1 x \tag{2.3}$$

Similarly, state and output equation for the other types of the converter can be obtained. These are given in Appendix A.1. Now refer to Fig. 2.1. Suppose the state and input matrices between the instants t_0 and t_1 for a converter are A_1 and B_1 respectively. The system dynamics in the interval $t_0 \le t < t_1$ is

$$\frac{dx}{dt} = A_1 x + B_1 V_{dc} \tag{2.4}$$

Similarly if the state and the input matrices respectively be A_2 and B_2 in the interval $t_1 \le t < t_2$, we get

$$\frac{dx}{dt} = A_2 x + B_2 V_{dc} \tag{2.5}$$

It is to be noted that $t_1 - t_0 = dT$ and $t_2 - t_1 = (1-d)T$ and state variable is continuous.

The solution of (2.4) for a given initial condition $x(t_0)$ is given by [61]

$$x(t_1) = e^{A_1(t_1 - t_0)} x(t_0) + \int_{t_0}^{t_1} e^{A_1(t-\tau)} B_1 V_{dc} d\tau$$

Since $t_1 - t_0 = dT$, we can write the above equation as

$$x(t_1) = \Phi_1 x(t_0) + \Theta_1 V_{dc} \tag{2.6}$$

where $$\Phi_1 = e^{A_1 dT} \tag{2.7}$$

and $$\Theta_1 = \int_0^{dT} e^{A_1(dT-\tau)} B_1 \, d\tau \tag{2.8}$$

Noting that $t_2 - t_1 = (1-d)T$, the solution of (2.5) is given by

$$x(t_2) = \Phi_2 x(t_1) + \Theta_2 V_{dc} \tag{2.9}$$

where $$\Phi_2 = e^{A_2(1-d)T} \tag{2.10}$$

$$\Theta_2 = \int_0^{(1-d)T} e^{A_2((1-d)-\tau)} B_2 \, d\tau \tag{2.11}$$

Combining (2.6) and (2.9), we can find the state at the time t_2, for a given duty ratio, d and the value of the state at time t_0 as

$$x(t_2) = \Phi_2\Phi_1 x(t_0) + (\Phi_2\Theta_1 + \Theta_2)V_{dc} \tag{2.12}$$

All the matrices Φ_2, Φ_1, Θ_2 and Θ_1 depend on the duty ratio. Hence $x(t_2)$ is a function of the duty ratio only for a constant supply voltage V_{dc} and the switching frequency only. The dc-dc converter is switched on at t_0 and then again at t_2. Therefore, at the steady state we have $x(t_2) = x(t_0) = x_0$. This value can be obtained from (2.12) for a given duty ratio as

$$x_0 = x(t_2) = \left[I - \Phi_2\Phi_1\right]^{-1}(\Phi_2\Theta_1 + \Theta_2)V_{dc} \tag{2.13}$$

Before we proceed with the derivation of the perturbation model, it is important to consider the steady state characteristics of a dc-dc converter. The steady state waveforms for a Buck-Boost converter are shown in Fig. 2.5. It can be seen from this figure that the output voltage falls and inductor current rises at the instants when the switch is closed. We define these points as corner points (CP) or the end points. The value of the state variables can be defined either at these corner points or the average value between two successive corner points.

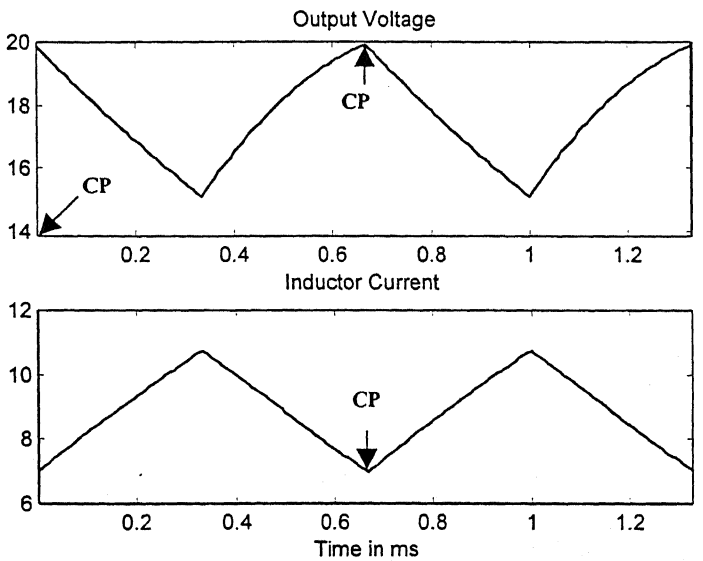


Fig. 2.5 Voltage and Current waveforms of Buck-Boost converter at 0.5 duty ratio.

As mentioned earlier, for a constant dc input voltage V_{dc}, the output voltage V_0 can only be changed by adjustment of duty ratio d of the control switch. The duty ratio is the control or the input variable in control engineering terminology. This quantity appears in state transition matrices Φ_2, Φ_1 and in the input matrices Θ_2 and Θ_1 as well. As a state transition matrix (STM) is an exponential of state matrix, the relation between input (d) and the output V_0 is nonlinear. Thus, design of controller requires linearization of converter dynamic model given in (2.12).

2.2 PERTURBATION MODELS FOR CONVERTERS IN CCM

The perturbation model of a dc-dc converter has been derived by Taylor's series expansion of the converter equation given in (2.12). This expansion has infinite number of terms and thus requires truncation for obtaining a model, which can be then used for controller design.

Let us consider a function $z = f(x, y)$ of two variables x and y. Let small perturbations in x and y cause small perturbation in z. Thus, if $(x = x_0 + \tilde{x}, y = y_0 + \tilde{y})$, then $z = z_0 + \tilde{z} = f(x,y)|_{x=x_0, y=y_0} + \tilde{f}(x,y)$. The quantities $(\tilde{x}, \tilde{y})$ are said to be small perturbation in variables (x, y) around the nominal point (x_0, y_0). By Taylor's series expansion theorem [62], we can write

$$\begin{aligned}\tilde{f}(x,y) = f(x_0+\tilde{x}, y_0+\tilde{y}) \; - f(x_0,y_0) \;\; = \\ = \left[\tilde{x}\frac{\partial}{\partial x} f(x,y)|_{x_0,y_0} + \tilde{y}\frac{\partial}{\partial y} f(x,y)|_{x_0,y_0}\right] \\ + \frac{1}{2!}\left[\tilde{x}^2\frac{\partial^2}{\partial x^2} f(x,y)|_{x_0,y_0} + 2\tilde{x}\,\tilde{y}\frac{\partial^2}{\partial y \partial x} f(x,y)|_{x_0,y_0} + \tilde{y}^2\frac{\partial^2}{\partial y^2} f(x,y)|_{x_0,y_0}\right] \\ + \cdots\cdots\cdots\end{aligned} \tag{2.14}$$

Now refer to equation (2.12). For this equation the independent variables are $x(t_0)$ and d. Thus we can obtain a perturbation model of $x(t_2)$ around a nominal operating point $x(t_0)$ and d_0. This is discussed below.

2.2.1 Linear Perturbation model of Converter in CCM

Let us rewrite (2.12) as

$$x(t_2) = \Phi_2\Phi_1 x(t_0) + (\Phi_2\Theta_1 + \Theta_2)V_{dc} \tag{2.15}$$

where Φ_1, Φ_2, Θ_1 and Θ_2 are the matrices evaluated at d_0. The Taylor's series expansion of (2.15) while truncating 2nd and higher order terms yields

$$\tilde{x}(t_2) = F\tilde{x}(t_0) + G\tilde{d} \tag{2.16}$$

where $$F = \frac{\partial x(t_2)}{\partial x(t_0)} \text{ and } G = \frac{\partial x(t_2)}{\partial d}$$

The actual expressions of these matrices are given in Appendix A.2.

Let the instant t_0 be the reference instant k that coincides with the closing of the switch. The instant t_2 then can be defined as (k+1), where $k = 0,1,2,.....$ is the discrete time index. We can therefore express equation (2.16) in discrete time state space form as

$$\tilde{x}(k+1) = F\tilde{x}(k) + G\tilde{d}(k) \tag{2.17}$$

The output equation is given by

$$\tilde{y}(k) = C\tilde{x}(k) \tag{2.18}$$

Equation (2.17) is called the Linear Perturbation Model (LMP) of the converter.

2.2.2 Bilinear Corner Point Perturbation (BCP) Model

The linear model is obtained by neglecting the second and higher order terms of (2.14) in the expansion of (2.15). If in addition to the first two terms of (2.14), we include the second order product term, the resulting equation is called Bilinear Corner Point (BCP) perturbation model. In this case, we obtain a modified form of (2.17), which includes the bilinear term.

$$\tilde{x}(k+1) = F\tilde{x}(k) + G\tilde{d}(k) + H\tilde{x}(k)\tilde{d}(k) \tag{2.19}$$

where F & G are the same as in the linear case and H is given by

$$H = \frac{\partial^2 x(t_2)}{\partial d \partial x(t_0)}$$

From (2.12) we get

$$H = \frac{\partial(\Phi_2\Phi_1)}{\partial d} = \frac{\partial(\Phi_2)}{\partial d}\Phi_1 + \Phi_2 \frac{\partial(\Phi_1)}{\partial d} = -A_2 T \Phi_2 \Phi_1 + \Phi_2 A_1 T \Phi_1 \qquad (2.20)$$

The output equation (2.18) also remains valid for the BCP model.

2.2.3 Model Verification

In this section, simulation results of some of the dc-dc converters, namely Buck, Boost, Buck-Boost and Cŭk converter, are presented to validate the perturbation models. The circuit diagram and dynamic equations of these converters are given in Appendix A.1. The converter operation is simulated by solving dynamic equations of the converter by ordinary differential equation solver routine available in MATLAB. The circuit parameters of different converters are listed in Table 2.1 along with the other test parameters.

First the system steady state condition for a given duty ratio is calculated from (2.13). The system simulation is then started with these nominal state values (x_0). To obtain perturbed quantities, the duty ratio is changed and the state variables are measured at each subsequent corner point. The actual perturbed system quantities are then obtained by subtracting the nominal state value (x_0) from measured state variables from the simulation. We shall call this "Simulated System Perturbation" or **SSP**. To obtain the predicted state values, we first calculate the matrices F, G and H based on (x_0) and d_0 from the results of Appendix A.2 and (2.20). The response of the Linear Model Prediction (**LMP**) calculated from (2.17) or the Bilinear Model Prediction (**BMP**) calculated from (2.19) is then recorded by giving step input $\tilde{d} = d - d_0$ to these models. The summary of the simulation results are presented in this section are listed in Table 2.1.

These simulation studies are carried out at a switching frequency close to that of the circuit natural frequency. Generally small signal model are validated at higher frequency

compared to natural frequency [15]. The model prediction error goes up with decrease in frequency. If the prediction error of the proposed model is acceptable at a lower frequency, the superiority of the model is established. The natural frequencies of the converters (imaginary part of the eigenvalues of matrices A_1 and/or A_2) taken for simulation and experimental verification is approximately 1000 Hz, therefore the switching frequency of converters are taken to be 1500 Hz. The model performance will better at higher frequency for the same component values.

Table 2.1 Summary of Simulation study of Corner Point Perturbation Models

Name of Converter	d_0	$\tilde{d}$	Circuit Parameters	Result Shown in Fig. No.
Buck Converter	0.3	0.6	$f = 1500Hz \;\; R = 5\Omega$ $L = 3mH \;\; C = 300\mu F \;\; V_{dc} = 20V$	Fig. 2.6
Boost Converter	0.3	0.3	$f = 1500Hz \; ; \; R = 10\Omega \;\; L = 4mH$ $C = 330\mu F \;\; V_{dc} = 20V$	Fig. 2.7
Cuk Converter	0.3	0.3	$L_1 = 50mH \;\; L_2 = 10mH \;\; C = 100\mu F$ $C_1 = 680\mu F \;\; R = 10\Omega \;\; V_{dc} = 20V$	Fig. 2.8
Buck-Boost Converter	0.3	0.1	$f = 1500Hz \;\; R = 5\Omega$ $L = 3mH \;\; C = 300\mu F \;\; V_{dc} = 20V$	Fig. 2.9
Buck-Boost Converter	0.3	0.3	Same as above	Fig. 2.10
Buck-Boost Converter	0.3	0.4	Same as above	Fig. 2.11
Buck-Boost Converter	0.5	-0.2	Same as above	Fig. 2.12

Please note that the simulation results use the following convention. The simulated system perturbation (SSP) is shown by solid lines, the linear model prediction (LMP) is shown by dotted lines and the bilinear model prediction (BMP) is shown by alternate dash and dots.

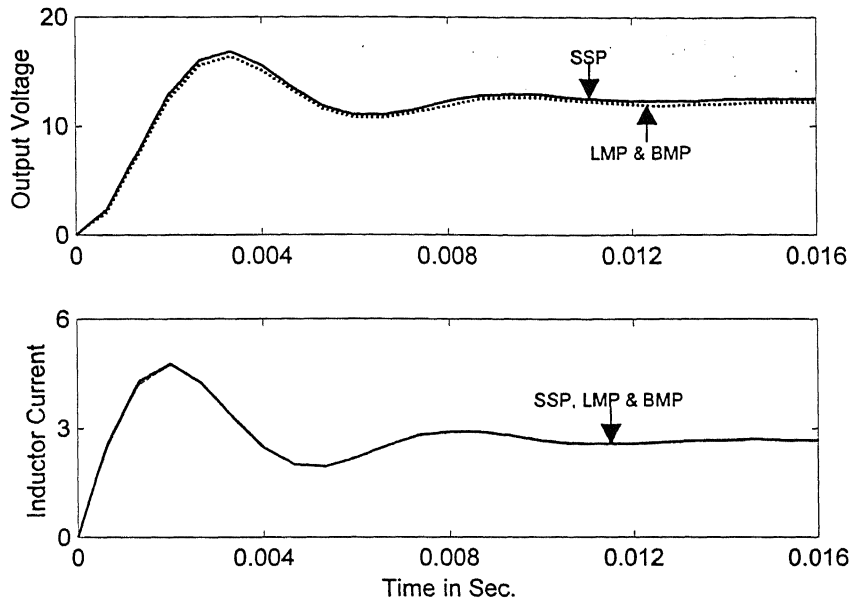


Fig.2.6: Simulation of perturbation modeling for a Buck converter when a step change of $\tilde{d} = 0.6$ in duty is made at $d_0 = 0.3$.

The dynamics of output voltage and inductor current of a Buck converter in transient as predicted by linear and bilinear corner point prediction model is shown in Fig. 2.6. It can be seen from the figure that predicted waveform matches closely with the simulated system perturbation (SSP) waveform. The performance of BCP model is marginally better than linear CP model in this case. The steady state error in the output voltage for both the models are significantly small whereas the error in inductor current is almost zero. This is why the inductor waveform looks as a single curve. It is to be noted that a $\tilde{d}$ is 0.6 for a nominal duty of $d_0 = 0.3$, is a significantly large perturbation.

In the similar way, the dynamics of output voltage and inductor current of a Boost converter as predicted by linear and bilinear corner point prediction model is shown in Fig. 2.7. It can be seen from the figure that the bilinear model prediction is not as good as in the

case of the Buck converter. Nevertheless, the prediction is within the acceptable limits and far better then linear prediction model.

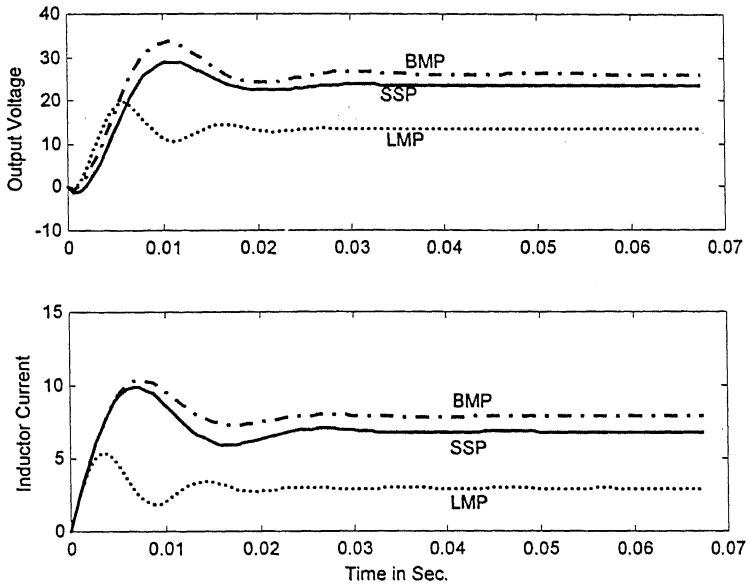


Fig.2.7: Simulation of perturbation modeling for a Boost converter when a step change of $\tilde{d} = 0.3$ in duty is made at $d_0 = 0.3$

Let us take a converter, which has more than two state variables. Cŭk has four states variable. The circuit diagram and its relevant dynamic equations are given in Appendix A.1. It is desired to model the perturbation of states of the Cŭk converter. The perturbation of simulated state variables and their prediction by LMP and BCP models are shown in Fig. 2.8. The BCP model prediction is close enough to the simulated system perturbation (SSP). Linear CP model has a poor performance in both transient and steady state. The steady state error is significant.

The Buck-Boost converter has been chosen for detailed study in the following chapters. Therefore a detailed simulation study is performed for this converter. The results are shown in Fig. 2.9 to Fig. 2.12. The parameters of the converter are given in Table 2.1. The perturbation in duty $\tilde{d}$ is varied from 0.2 to 0.4 at a nominal duty ratio of 0.3. It can be seen from these simulation studies that BCP model predicts better than linear CP model. The range of the perturbation in duty ratio for which the prediction by BCP model is acceptable is quite large.

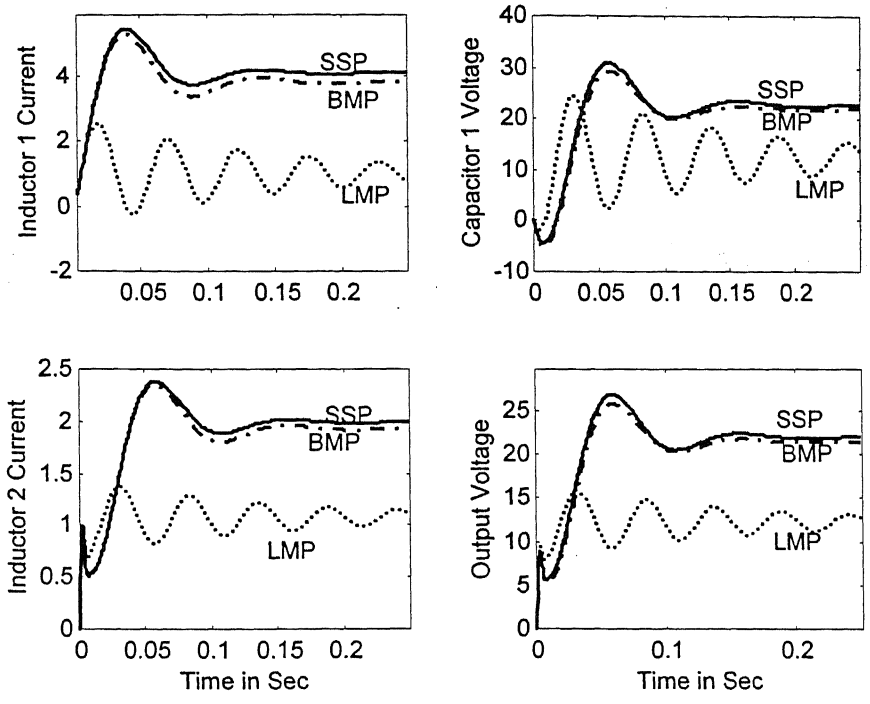


Fig.2.8: Simulation of perturbation modeling for a Cŭk converter when a step change of 0.2 in duty is made at 0.3.

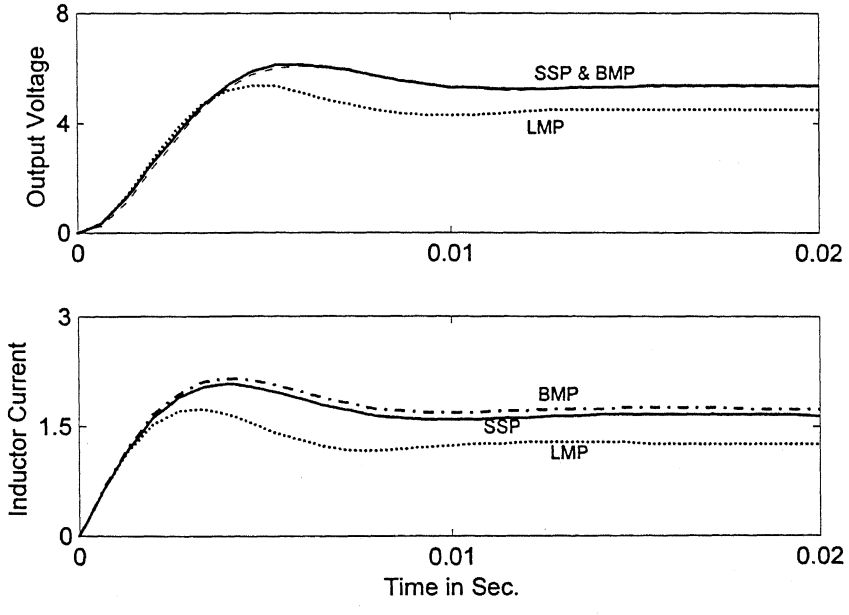


Fig.2.9: Simulation of perturbation modeling for a Buck-Boost converter when a step change of $\tilde{d} = 0.1$ in duty is made at $d_0 = 0.3$

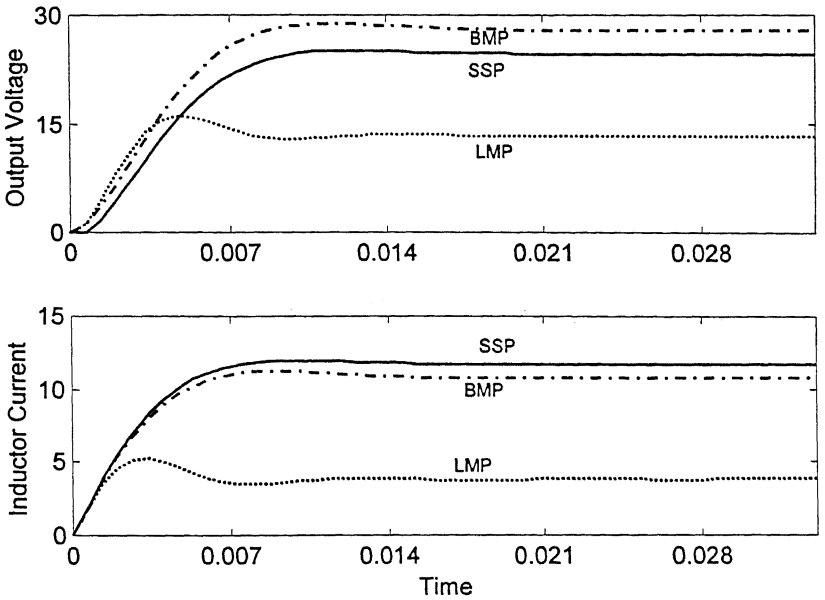


Fig.2.10: Simulation of perturbation modeling for a Buck-Boost converter when a step change of $\tilde{d} = 0.3$ in duty is made at $d_0 = 0.3$

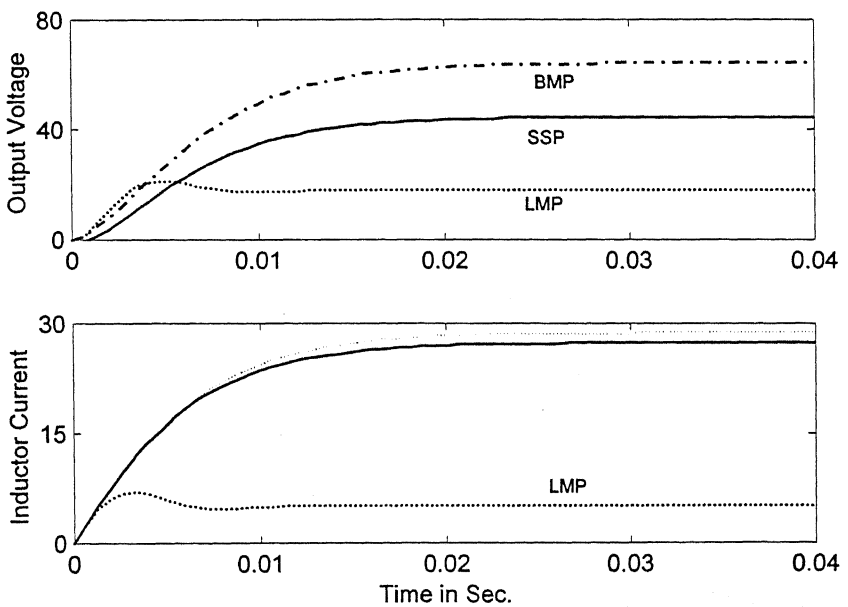


Fig.2.11: Simulation of perturbation modeling for a Buck-Boost converter when a step change of $\tilde{d} = 0.4$ in duty is made at $d_0 = 0.3$

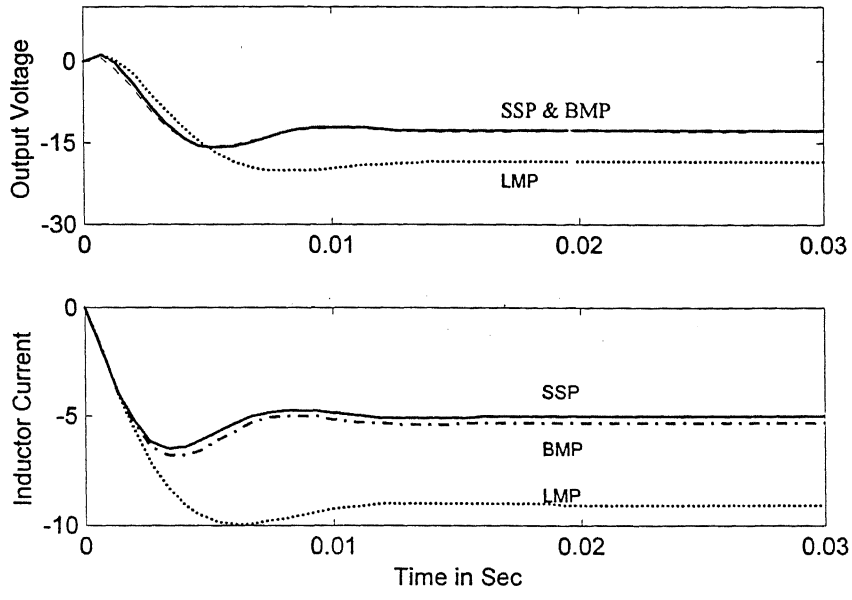


Fig.2.12: Simulation of perturbation modeling for a Buck-Boost converter when a step change of $\tilde{d} = -0.2$ in duty is made at $d_0 = 0.5$

Fig. 2.12 shows simulation for negative perturbation in duty ratio. An attempt to apply a positive perturbation in duty ratio larger than 0.4 results in model failure. The reason for this is explained as follows. Consider the bilinear model of (2.19). For a fixed $\tilde{d}$ this is given as

$$\tilde{x}(k+1) = \left(F + H\tilde{d}\right)\tilde{x}(k) + G\tilde{d}(k) = M\tilde{x}(k) + G\tilde{d}(k) \tag{2.21}$$

If $\tilde{d}$ is large then the eigenvalues of the matrix M may be outside the unit circle. This will make the prediction model unstable and both the output voltage and inductor current will become unbounded. The linear model of (2.17) does not suffer from this problem of instability even though the steady state errors for large perturbation will be very large. This observation with bilinear model shows a limiter must be placed along with a controller, which may be designed based on the bilinear model, to limit the value of $\tilde{d}$ to prevent instability.

To illustrate this we consider the bilinear model of the Buck-Boost converter for a nominal duty ratio of 0.3 and a perturbation of duty ratio ($\tilde{d}$) of 0.6. The eigenvalues of the matrix M in (2.21) are computed with the change in converter frequency. These are

shown in Fig. 2.13. It can be seen that one of the eigenvalues is unstable (greater than 1.0) in the lower frequency range. It however becomes stable, even though marginally, at the higher frequency range.

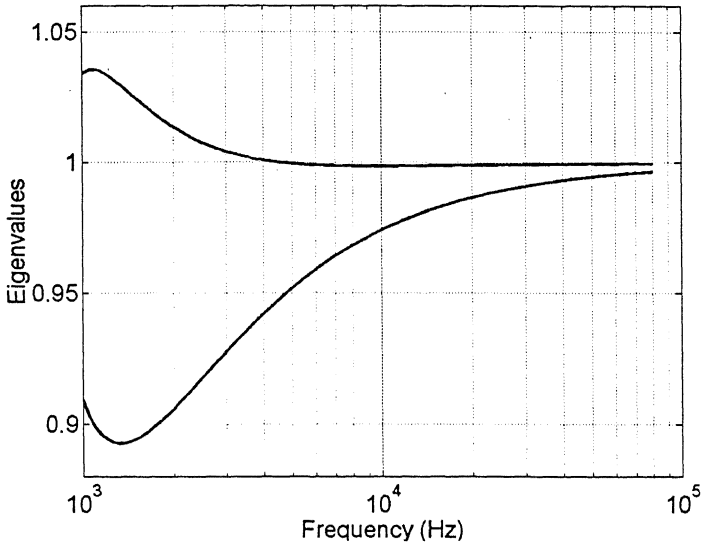


Fig. 2.13 Plot of the eigenvalues with the change in frequency of the Buck-Boost converter for $d = 0.3$ & $\tilde{d} = 0.6$

The results discussed so far are with models that are derived at much lower frequency. The amount of the error shown above in the simulation looks significant but for a converter running at higher frequency this error will be small.

In this section we have derived discrete-time models for the corner points. The same technique can also be used for deriving models that characterizes the perturbations in the average quantities over a cycle. This is discussed in the next section.

2.3 AVERAGED STATE MODEL

Obtaining an averaged perturbation model begins with finding an equation for the average states over a switching cycle. This equation is then represented by infinite terms of Taylor's series. Truncation of infinite series gives various perturbation models. Since no approximation has been made before perturbation, the model that will be derived using this method will have obvious advantage over other averaged models such as State Space

Averaging (SSA) Method of [15]. In this section we shall derive the model and demonstrate that the proposed averaging method has better accuracy at lower frequency as well as at higher frequency. Before we introduce the proposed averaging method, let us briefly discuss the SSA model.

2.3.1 The SSA Model

The state space averaging method uses average description of the state equation. If we assume the ripple in the current and voltage to be small, then the states over a cycle can be assumed to be constant. As the states are assumed constant, the dynamic equation of the average state is given by

$$\frac{dx}{dt} = [A_1 d + A_2(1-d)]x + [B_1 d + B_2(1-d)]V_{dc} \tag{2.22}$$

Similarly, the assumption of low ripple allows one to write the output equation as

$$V_o = [C_1 d + C_2(1-d)]x \tag{2.23}$$

Using these above relation small perturbation model can be derived by Taylor's series expansion of the above equation around a nominal point. The small signal model by this method is given by (2.24).

$$\frac{d\tilde{x}}{dt} = [A_1 d + A_2(1-d)]\tilde{x} + [(A_1 - A_2)X_0 + (B_1 - B_2)V_{dc}]\tilde{d} \tag{2.24}$$

2.3.2 Proposed averaging method

The average of the state variables are obtained by integrating the solution of the state space equation over a switching cycle and dividing it by the time period. Let x_{av} be the average value of the state over one cycle, then

$$x_{av} = \frac{1}{T}\int_0^T x(t)dt = \frac{1}{T}\left[\int_0^{dT} x_1(t)dt + \int_{dT}^{T} x_2(t)dt\right] \tag{2.25}$$

where $x_1(t)$ and $x_2(t)$ are given by the following equations.

$$x_1(t) = e^{A_1(t-t_0)}x(t_0) + \int_{t_0}^{t} e^{A_1(t-\tau)}B_1 V_{dc}\,d\tau$$

$$x_2(t) = e^{A_2(t-t_0)}x(t_1) + \int_{t_0}^{t} e^{A_2(t-\tau)}B_2 V_{dc}\,d\tau$$

The above equations when substituted in (2.14) and integrated using the results of Appendix A.3 give the following expression for the average state.

$$\begin{aligned} Tx_{av} &= \left[A_1^{-1}(e^{A_1 dT} - I) + A_2^{-1}e^{A_2 dT}(e^{A_2(1-d)T} - I)\right]x(t_0) \\ &+ \left[\left(A_1^{-1}\right)^2(e^{A_1 dT} - I)B_1 - \left(A_1^{-1}\right)dTB_1 + \left(A_2^{-1}\right)(e^{A_2(1-d)T} - I)\left(A_1^{-1}\right)(e^{A_1 dT} - I)B_1 \right. \\ &\left. + \left(A_2^{-1}\right)^2 e^{A_2 dT}(e^{A_2 dT} - I)B_2 - \left(A_2^{-1}\right)(1-d)TB_2\right]V_d \end{aligned} \quad (2.26)$$

The above solution is valid for converters having nonsingular state matrix A_1 and A_2. For Singular matrices, exact calculation of product of matrices has to be carried by a method similar to that given for the corner point model in Appendix A.2.

2.3.3 Bilinear Average Model

The bilinear average model is derived by truncating the Taylor series expansion of the average equation of (2.26) and it is given by

$$\tilde{x}_{av}(t_2) = F_{av}\tilde{x}(t_0) + G_{av}\tilde{d} + H_{av}\tilde{x}(t_0)\tilde{d} \quad (2.27)$$

If instant t_0 is named the discrete time k^{th} instant then t_2 will be represented by $(k+1)^{th}$ instant. Substituting these, (2.27) can be written as (2.27a) in discrete time representation.

$$\tilde{x}_{av}(k+1) = F_{av}\tilde{x}(k) + G_{av}\tilde{d} + H_{av}\tilde{x}(k)\tilde{d} \quad (2.27a)$$

The $\tilde{x}_{av}(k+1)$ vector contains the average value of voltage and current over a switching cycle i.e. in the intervals from t_0 to t_2. It is to be noted that the average values are still defined in terms of the corner point variable, i.e. $\tilde{x}(k)$ and $\tilde{d}(k)$. Depending on the particular output variable, we then pre multiply $\tilde{x}_{av}(k)$ by appropriate row vector. For

example, if we define the averaged output voltage as the output variable, we pre multiply by row vector $C=[1 \quad 0]$. The matrices F_{av}, G_{av} and H_{av} of (2.26) for Buck-Boost converter are given in appendix A.3.

2.3.4 Linear Averaged Perturbation Model

For smaller perturbations in duty at higher switching frequency, the bilinear term of (2.27) can be neglected without incurring significant error in the model. This results in a model, which contains only linear terms and hence called the linearized average model. The Linear average perturbation model is given by

$$\tilde{x}_{av}(t_2) = F_{av}\tilde{x}(t_0) + G_{av}\tilde{d} \tag{2.28}$$

It is interesting to note that using (2.16) and (2.28), we can obtain a linear description between the perturbation in duty ratio and the output voltage or inductor current in interval t_0 and t_2. For example, defining a matrix C as $C=[1 \quad 0]$, we get

$$\frac{\tilde{v}_{oav}(z)}{\tilde{d}(z)} = z^{-1}\left[CF_{av}(zI-F)^{-1}G + CG_{av}\right] \tag{2.29}$$

We can then use the above equation to design a controller in frequency domain or polynomial domain.

2.3.5 Simulation Results

The Simulation study has been done to validate the averaged perturbation models. A Buck-Boost converter has been taken for this purpose. The parameters of the converter are same as for the simulation study done in Table 2.1, but it is reproduced below for convenience.

$$f = 1500\,Hz \;\; R = 5\Omega \;\; L = 3\,mH \;\; C = 300\,\mu F \;\; V_{dc} = 20V$$

Out of a number of simulations have been carried out for verification of the model, some of the representative simulation results presented in this subsection. These results are

summarized below in Table 2.2.

Table 2.2 Summary of Simulation study for verification of Averaged Perturbation modeling on Buck-Boost Converter

d_0	$\tilde{d}$	Result Shown in Fig.
0.3	0.1	Fig. 2.14
0.3	0.3	Fig. 2.15
0.3	0.4	Fig. 2.16
0.6	-0.2	Fig. 2.17

The simulation results are shown in Figs. 2.14 to 2.17. The converter is assumed to operate at 1500 Hz which is close to the natural frequency of the converter. The model performance is also compared with the SSA model for each case. The perturbation in duty for Fig. 2.14 is too small and hence the perturbed state and the predicted values show a close match. The bilinear perturbation model has larger steady state error compared to linear model. But the steady state error for a perturbation of 0.3 in duty ratio as shown in Fig. 2.15 with bilinear model is less compared its linear counterpart. The result shown in Fig. 2.16 is for $\tilde{d} = 0.4$ and steady state error is comparable. It can be seen in Fig. 2.17 that bilinear model has less error compared to all others for a negative perturbation. Since the converter can have both positive and negative perturbation, the average perturbation model that describes converter best is the bilinear average model discussed.

The Linear corner point, BCP and average prediction models are validated above at lower frequency. Normally the converters are operated at much higher frequency than its natural frequency. The converter model performance is therefore simulated at a switching frequency of 50KHz. The results are shown in Fig. 2.18 to 2.20 and results are summarized in Table 2.3.

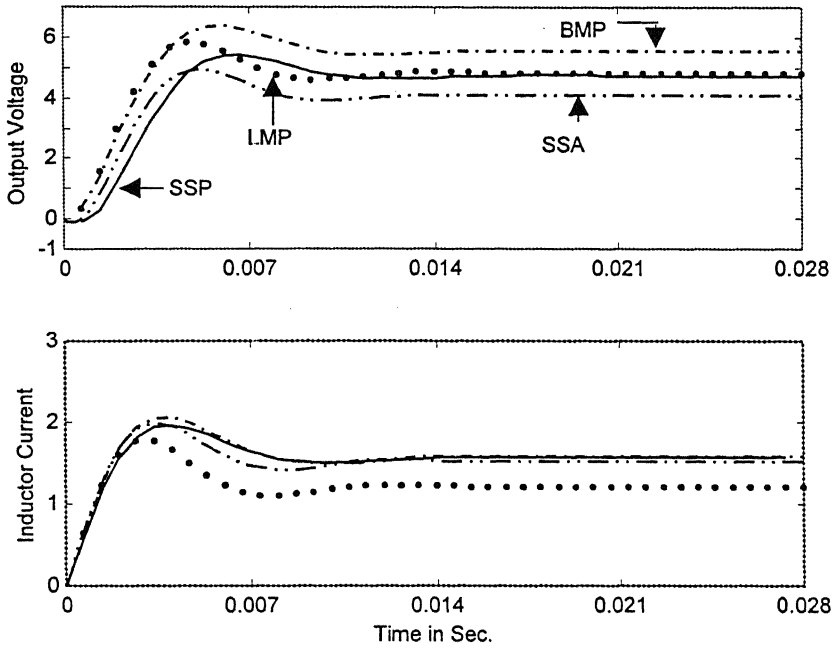


Fig. 2.14: Simulation of average perturbation modeling for a Buck-Boost converter for a step change of 0.1 in duty cycle at a steady state duty of 0.3.

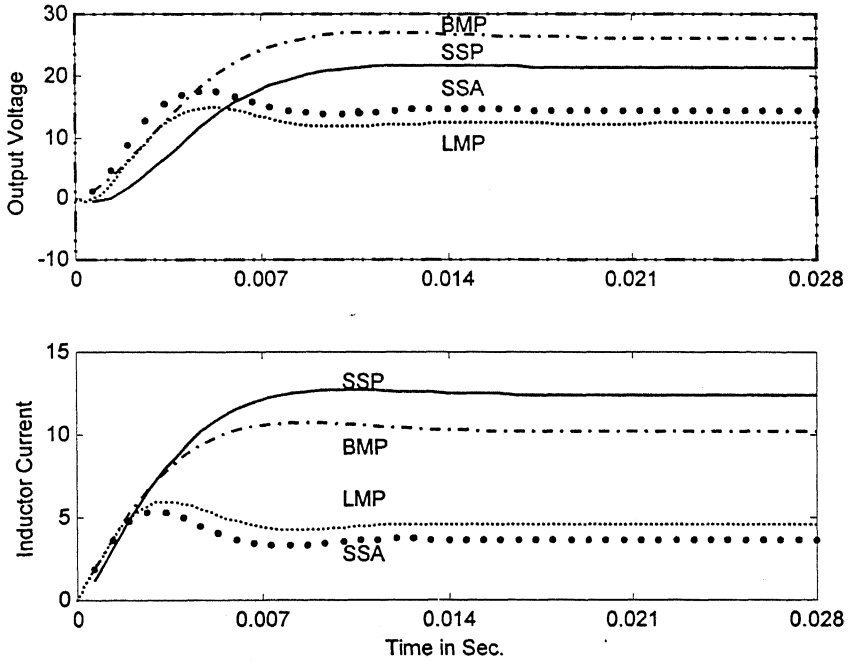


Fig. 2.15: Simulation of average perturbation modeling for a Buck-Boost converter for a step change of 0.3 in duty cycle at a steady state duty of 0.3.

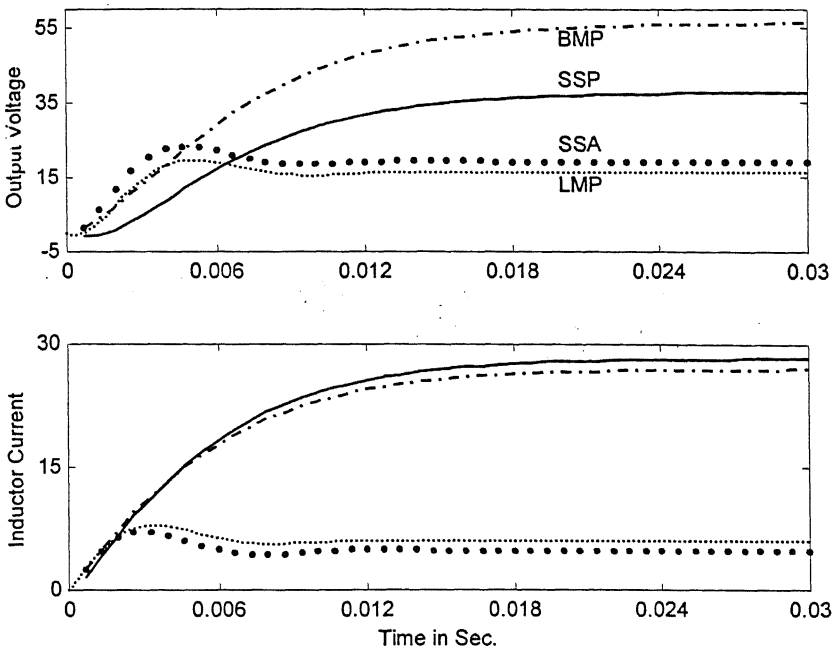


Fig. 2.16: Simulation of average perturbation modeling for a Buck-Boost converter for a step change of 0.4 in duty cycle at a steady state duty of 0.3.

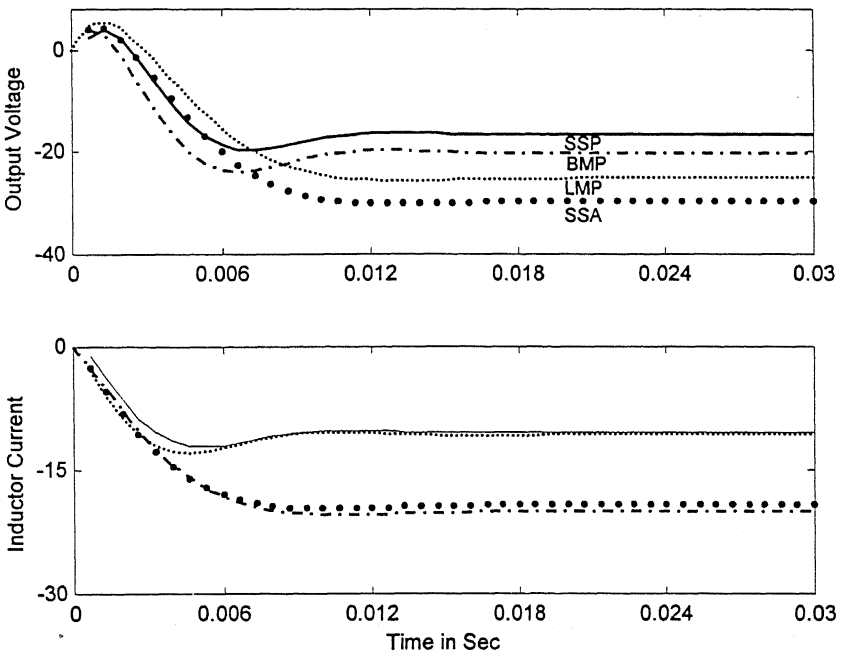


Fig. 2.17: Simulation of average perturbation modeling for a Buck-Boost converter for a step change of - 0.2 in duty cycle at a steady state duty of 0.6.

Table 2.3 Simulation Results at higher frequency

Converter	Model	d_0	$\tilde{d}$	Result shown in Fig.
Buck-Boost	Average Model	0.3	0.3	Fig 2.18
Buck-Boost	Corner Point	0.3	0.3	Fig 2.19
Buck	Corner Point	0.3	0.6	Fig 2.20

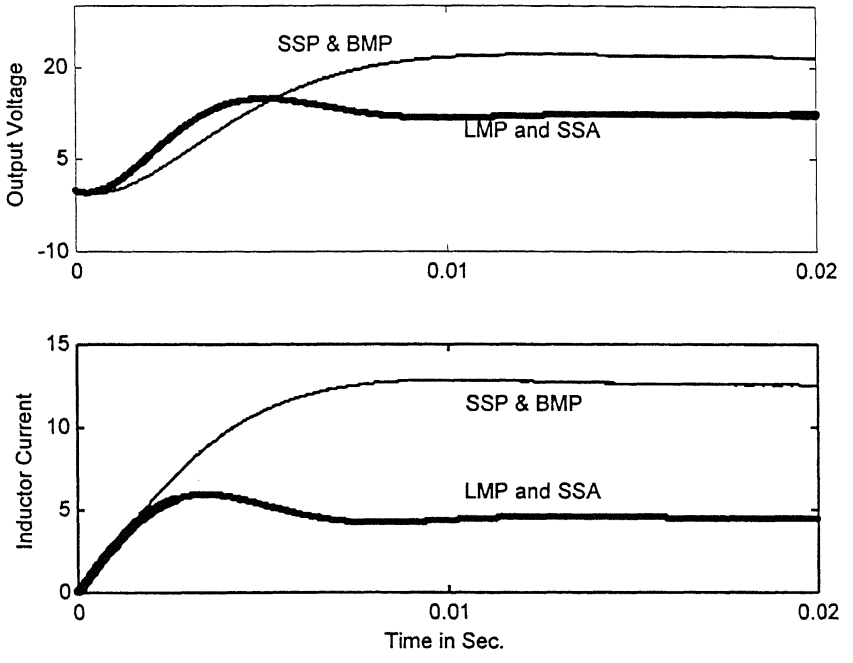


Fig. 2.18: Simulation of average perturbation modeling for a Buck-Boost converter for a step change of 0.3 in duty cycle at a steady state duty of 0.3.at 50 kHz.

It can be seen from Fig. 2.18 that the bilinear model and simulated actual perturbation becomes almost coincident whereas the linear and SSA model prediction is far below. Therefore the superiority of the bilinear average model is established. The corner point models shown in Figs. 2.19 and 2.20 show the similar advantage.

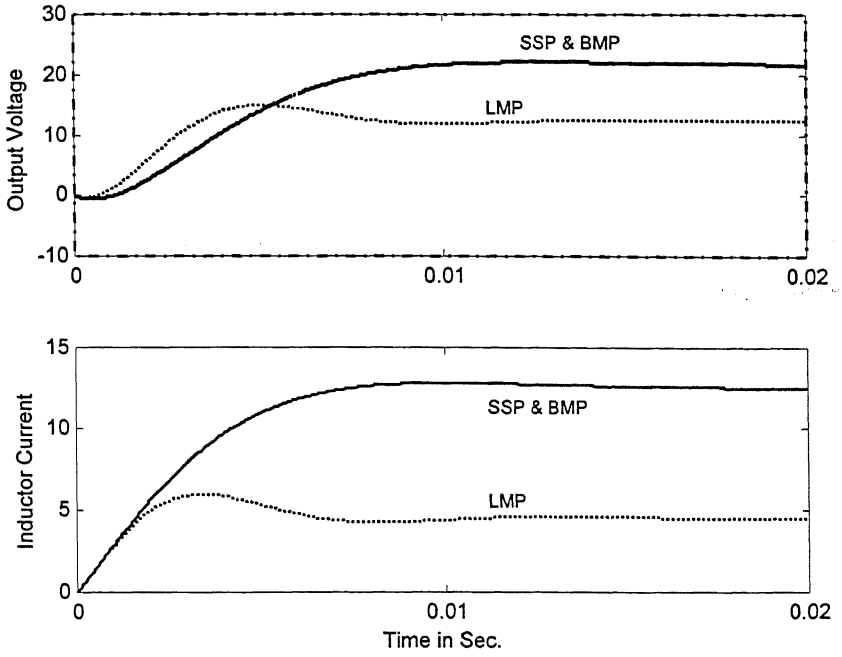


Fig. 2.19: Simulation of Corner point perturbation modeling for a Buck-Boost converter for a step change of 0.3 in duty cycle at a steady state duty of 0.3.at 50 kHz.

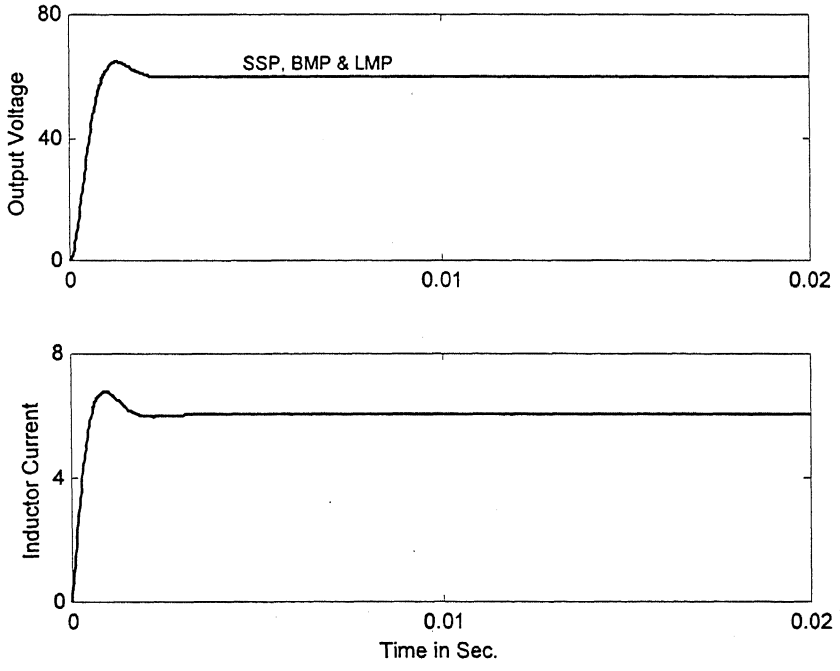


Fig. 2.20: Simulation of Corner point perturbation modeling for a Buck converter for a step change of 0.3 in duty cycle at a steady state duty of 0.6.at 50 kHz.

2.4 GENERALIZED CONVERTER MODEL IN CCM

In this section we shall derive a generalized perturbation model of a dc-dc converter from which all other models discussed before can be derived. For simplicity, we shall only consider the corner point prediction model of the converter. Let us assume that converter is operating in CCM at a duty ratio of d_0 and we now perturb it such that duty becomes $d_0 + \tilde{d}$. We then can write from (2. 6) and (2.9)

$$x'(t_1) = x(t_1) + \tilde{x}(t_1) = \Phi_1' x(t_0) + \Theta_1' V_{dc}$$

where

$$\left.\begin{aligned} \Phi_1' &= e^{A_1(d+\tilde{d})T} \\ \Theta_1' &= \int_0^{(d+\tilde{d})T} e^{A_1(t-\tau)} B_1 \, d\tau \end{aligned}\right\} \tag{2.30}$$

Similarly,

$$x'(t_2) = x(t_2) + \tilde{x}(t_2) = \Phi_2' x'(t_1) + \Theta_2' V_{dc} \tag{2.31}$$

where

$$\left.\begin{aligned} \Phi_2' &= e^{A_2[1-(d+\tilde{d})]T} \\ \Theta_2' &= \int_0^{[1-(d+\tilde{d})]T} e^{A_2(t-\tau)} B_2 \, d\tau \end{aligned}\right\}$$

Substituting (2.26) into (2.27) we get

$$x(t_2) + \tilde{x}(t_2) = \Phi_2' \Phi_1' [x(t_0) + \tilde{x}(t_0)] + (\Phi_2' \Theta_1' + \Theta_2') V_{dc} \tag{2.32}$$

Subtracting (2.12) from the above equation we get

$$\tilde{x}(t_2) = \Phi_2' \Phi_1' \tilde{x}(t_0) + (\Phi_2' \Phi_1' - \Phi_2 \Phi_1) x(t_0) + (\Phi_2' \Theta_1' - \Phi_2 \Theta_1 + \Theta_2' - \Theta_2) V_{dc} \tag{2.33}$$

We now proceed with the perturbation model derivation from this large signal model. It will be shown that the various models described in earlier sections can be derived from this by suitable approximation.

2.4.1 Linear and Bilinear Model Deduction

The models derived in the Subsections 2.2.1 and 2.2.2 can be directly deduced from (2.33). If we assume the perturbation in the duty is small then $\tilde{d}T$ is a very small quantity and therefore the Taylor's series expansion of the matrix $e^{A_1\tilde{d}T}$ can be approximated by linear terms only. That is,

$$e^{A_1\tilde{d}T} = I + A_1\tilde{d}T$$

Thus, $$\Phi_1' = e^{A_1(d+\tilde{d})T} = e^{A_1\tilde{d}T}e^{A_1dT} \cong (I + A_1\tilde{d}T)\Phi_1 = \Phi_1 + A_1\Phi_1\tilde{d}T$$

Similarly, $$\Phi_2' \cong \Phi_2 - A_2\Phi_2\tilde{d}T$$

Proceeding in the similar way, we can show that

$$\Theta_1' = \Theta_1 + \Phi_1 B_1\tilde{d}T$$

and $$\Theta_2' = \Theta_2 - \Phi_2 B_2\tilde{d}T$$

With this linear approximation of the terms shown above, we can write from (2.29),

$$\begin{aligned}\tilde{x}(t_2) &= \Phi_2'\Phi_1'\tilde{x}(t_0) + (\Phi_2'\Phi_1' - \Phi_2\Phi_1)x(t_0) + (\Phi_2'\Theta_1' - \Phi_2\Theta_1 + \Theta_2' - \Theta_2)V_{dc} \\ &= [(\Phi_2 - A_2\Phi_2\tilde{d}T)(\Phi_1 + A_1\Phi_1\tilde{d}T)]\tilde{x}(t_0) \\ &\quad + \left[(\Phi_2 - A_2\Phi_2\tilde{d}T)(\Phi_1 + A_1\Phi_1\tilde{d}T) - \Phi_2\Phi_1\right]x(t_0) \\ &\quad + \Xi V_{dc}\end{aligned}$$

where

$$\begin{aligned}\Xi &= \Phi_2'\Theta_1' - \Phi_2\Theta_1 + \Theta_2' - \Theta_2 \\ &= (\Phi_2 - A_2\Phi_2\tilde{d}T)(\Theta_1 + \Phi_1 B_1\tilde{d}T) - \Phi_2\Theta_1 + \Theta_2 + \Phi_2 B_2\tilde{d}T - \Theta_2 \\ &= \Phi_2\Phi_1 B_1\tilde{d}T - A_2\Phi_2\tilde{d}T\Theta_1 - A_2\Phi_2\tilde{d}T\Phi_1 B_1\tilde{d}T + \Phi_2 B_2\tilde{d}T\end{aligned}$$

The above equation reduces on simple algebraic simplification to bilinear corner point (BCP) prediction model given by (2.19) if the terms containing T^2 in the above expansion are neglected. This will be true if T is very small or accompanying product term $\tilde{d}$ is very small. Thus, the model behavior is very good if the frequency of operation of the converter is either very high or perturbation in the duty ratio is very small. Dropping the bilinear term of the bilinear model results in linear model given in (2.17). It is interesting to note that the only approximation made in deriving the BCP prediction model is for the terms $e^{A_1\tilde{d}T}$ and $e^{A_2(1-\tilde{d})T}$ of the actual large signal prediction model, which requires $A_1^2\tilde{d}^2T^2 << [I]$ and $A_2^2(1-\tilde{d})^2T^2 << [I]$ where $[I]$ is identity matrix. Using these constraints, zone of validity for given frequency and circuit parameters can be obtained.

2.4.2 SSA Model Deduction

From the large signal perturbation model it is possible to deduce the state space model of the converters. If the frequency of operation of the converter is high enough, the quantity T is significantly small and thus, the whole term $e^{A_1(d+\tilde{d})T}$ can be linearly approximated without incurring large error. That is,

$$e^{A_1(d+\tilde{d})T} = I + A_1(d+\tilde{d})T$$

Neglecting the square terms (2.33) can be simplified to

$$\begin{aligned}\tilde{x}(t_2) &= \Phi_2'\Phi_1'\tilde{x}(t_0) + (\Phi_2'\Phi_1' - \Phi_2\Phi_1)x(t_0) + (\Phi_2'\Theta_1' - \Phi_2\Theta_1 + \Theta_2' - \Theta_2)V_{dc} \\ &= [I + A_2(1-d-\tilde{d})T][I + A_1(d+\tilde{d})T]\tilde{x}(t_0) \\ &+ \left[[I + A_2(1-d-\tilde{d})T][I + A_1(d+\tilde{d})T] - [I + A_2(1-d)T][I + A_1dT]\right] \\ &+ \aleph\end{aligned}$$

where $$\aleph = \Phi_2'\Theta_1' - \Phi_2\Theta_1 + \Theta_2' - \Theta_2$$

To simplify this we require evaluation of Θ in the above expression. This can written for high frequency as

$$\Theta_1 = A_1^{-1}[\Phi_1 - I]B_1 = A_1^{-1}[I + A_1dT - I]B_1 = B_1dT$$

Similarly, we can write

$$\Theta_1' = B_1(d+\tilde{d})T$$

and

$$\Theta_2' = B_2(1-d-\tilde{d})T$$

Substituting these values in equation for $\aleph$ given above,

$$\begin{aligned}\aleph &= [I + A_2(1-d-\tilde{d})T][B_1(d+\tilde{d})T] - [I + A_2(1-d)T][B_1 dT] \\ &\quad + B_2(1-d-\tilde{d})T - B_2(1-d)T \\ &= B_1\tilde{d}T - B_2\tilde{d}T\end{aligned}$$

Simple algebraic simplification lead to classical State space model of the converter. The averaging theorem has been extensively used in the modeling [19-23]. Essentially these methods provide a systematic way to select the expansion terms of the perturbation model derived using Taylor's series expansion of the large signal model. However, one can derive different small signal perturbation models by using appropriate approximations of (2.33).

2.5 GENERALIZED MODEL FOR MULTIPLE SUBINTERVALS

We have concentrated till now on small signal model of the converter, which have one controlled switch and one diode and operating in CCM. This is to say that there are just two modes or subintervals dT and $(1-d)T$ in a switching cycle. A converter in DCM has three subintervals. Similarly, the minimum number of subintervals (occurring in its CCM mode) in a switching cycle is equal to the number of controlled switching elements plus one for a converter with more than one controlled switching devices. One of the examples for such converter is modified flyback converter discussed in Chapter 4. In this section we derive a model for converters having more than two subintervals. Extension of the derivation of Section 2.4 for multiple subintervals results in generalized model.

Let there be n subintervals and $A_1, A_2, \cdots\cdots, A_n$ and $B_1, B_2, \cdots\cdots, B_n$ be the state and the input matrices in these subintervals. The perturbation model derived from the Taylor's series expansion method in the similar way as done in previous section. The perturbation of the n^{th} subinterval in terms of the perturbation of state in the beginning of

the cycle can be written as follows. In this expansion second and higher order terms except the bilinear term is neglected.

$$\tilde{x}(t_n) = \prod_{i=1}^{n}[\Phi_i']\tilde{x}(t_0) + \left[\prod_{i=1}^{n}\Phi_i' - \prod_{i=1}^{n}\Phi_i\right]x(t_0) + \sum_{j=1}^{n}\left(\prod_{j=1}^{n-j}\Phi_i'\Theta_j' - \prod_{j=1}^{n-j}\Phi_i\Theta_j\right)V_{dc}$$

where, $\prod_{i=1}^{n}[\Phi_i'] = \Phi_n'\Phi_{n-1}'\Phi_{n-2}'\cdots\cdots\Phi_1'$, $\sum_{j=1}^{n}\left(\prod_{j=1}^{n-j}\Phi_i'\Theta_j'\right) = \sum_{j=1}^{n}\Phi_{(n-j)}'\Phi_{(n-j-1)}'\cdots\cdots\Phi_1'\Theta_j$

and $\Phi_0 = I$

Using this model, we will derive the small signal perturbation model of modified Buck-Boost converter in Chapter 4.

2.6 EXPERIMENTAL VERIFICATION OF SIMULATION

In this section we shall present some experimental results and compare them with corresponding simulation results. It will be shown that the experimental results closely match simulation results. This implies that the experimental perturbation will match closely with the simulated system perturbation (SSP). Therefore the comparison of model given in the earlier sections is validated. The parameters of the converter used are given below. The experimental arrangements are described in detail in Chapter 6. The system parameters chosen are:

Inductor: $L = 3mH$, $R = 1.2\Omega$, Capacitor: $C = 330\mu F$, $esr = 20m\Omega$, Nominal Resistance $R = 64.04\Omega$, Frequency: $F = 26.076kHz$, DC Voltage: $V_{dc} = 10V$ *or* $20V$

The converter is first operated at a nominal (chosen arbitrarily) value of the duty ratio. This is followed by a perturbation in the duty from its nominal value. The transient in the inductor current and output voltage is recorded for a pre-calculated interval. This recording period should not be less than the settling time. Simulation of the converter with actual parameters is used to obtain an approximate value for this interval. The recording period has been taken nearly twice to this period in experiment in order to capture the complete transient. The actual values of the states (Inductor current and Capacitor Voltage)

are measured experimentally. We have carried out two sets of open loop simulations and experiments for two input voltages. This not only ensures the model validity at different input conditions, but also shows some interesting circuit behavior. The simulation and experimental results are summarized in Table 2.4.

Figs. 2.21 to Fig. 2.26 show the experimental and simulation results at input voltage of 10 V, while in Figs. 2.27 to 2.30 show the same when the input voltage is 20 V. In all these a step change in the duty ratio are made from their nominal values indicated. The dark noisy lines in the experimental curves shown in these figures are due to small switching oscillations when the switch undergoes a transition from ON state to OFF state and vice versa. The dark lines in the simulation studies are due to larger ripple in the output voltage and inductor current.

Table 2.4 Experimental verification of simulation

V_{dc}	d_0	$\tilde{d}$	Variable Under study	Result shown in Figure
10V	0.3	0.3	Output Voltage	Fig. 2.21
10V	0.3	0.3	Inductor Current	Fig. 2.22
10V	0.8	- 0.1	Output Voltage	Fig. 2.23
10V	0.8	-0.1	Inductor Current	Fig. 2.24
10V	0.2	0.4	Output Voltage	Fig. 2.25
10V	0.2	0.4	Inductor Current	Fig. 2.26
20V	0.3	0.2	Output Voltage	Fig. 2.27
20V	0.3	0.2	Inductor Current	Fig. 2.28
20V	0.2	0.4	Output Voltage	Fig. 2.29
20V	0.2	0.4	Inductor Current	Fig. 2.30

A perturbation of 0.3 in duty ratio at a nominal value of 0.3 is verified in Fig. 2.21 and Fig. 2.22 by experiment and simulation. The current waveform in experiment is peaky and steep compared to its simulation waveform. This can be attributed to saturation and stray capacitance of the inductor.

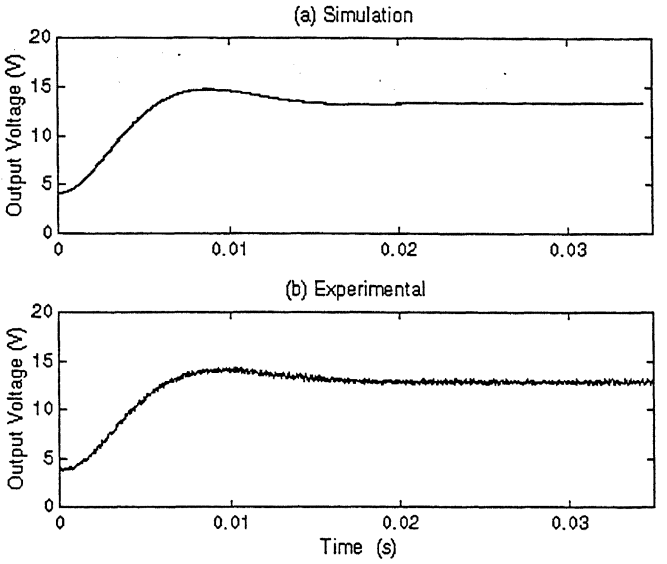


Fig. 2.21 Experimental and simulation result of Output Voltage for $d_0 = 0.3$ and $\tilde{d} = 0.3$

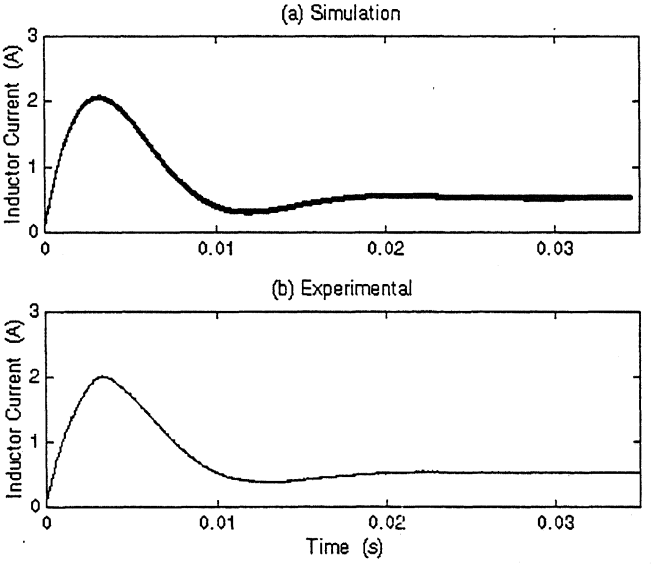


Fig. 2.22 Experimental and simulation result of Inductor Current for $d_0 = 0.3$ and $\tilde{d} = 0.3$

In an another study, a negative step change of 0.1 in duty from its nominal value of 0.8 is applied. The results are shown in Figs. 2.23 and 2.24. The voltage waveform matches

exactly with the simulation, but the current in simulation study goes zero before 0.0.005 s. This implies that the converter has entered a discontinuous conduction mode (DCM). However, the experimental curve does not indicate a DCM operation. This confirms that magnetic saturation is taking place as stated above.

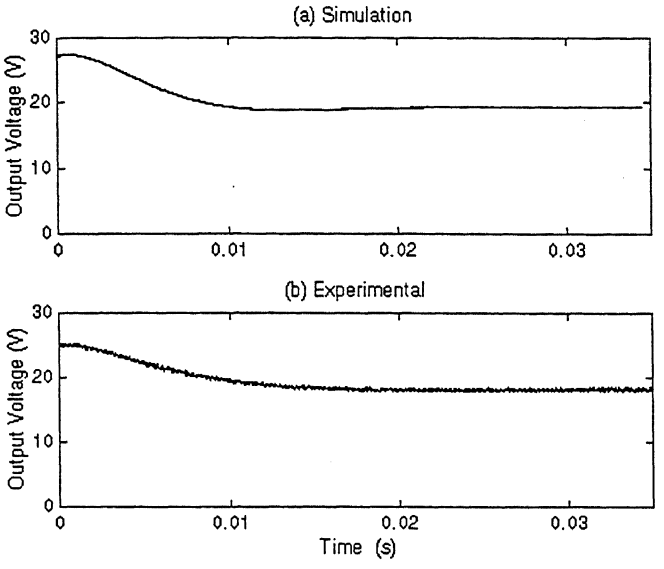


Fig. 2.23 Experimental and simulation result of Output Voltage for $d_0 = 0.8$ and $\tilde{d} = -0.1$

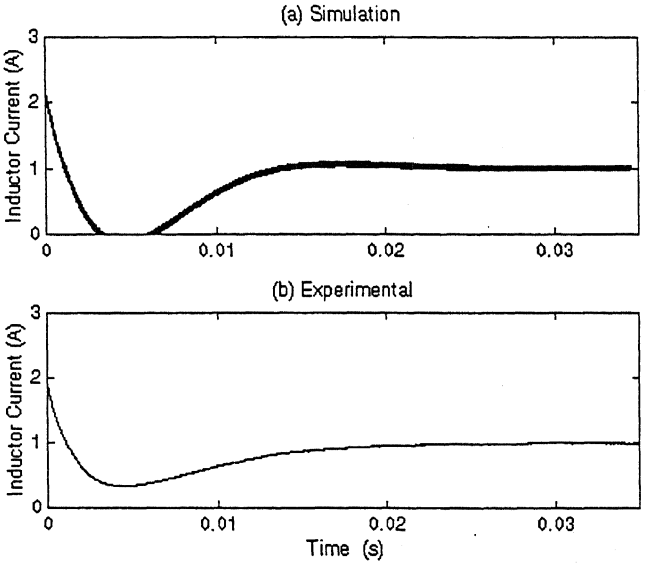


Fig. 2.23 Experimental and simulation result of Inductor Current for $d_0 = 0.8$ and $\tilde{d} = -0.1$

In order to validate the model for larger perturbations, a step change of 0.4 is applied when the converter is operating in nominal operating point of 0.2. The results are shown in

Figs. 2.25 and 2.26. The experimental and simulation results show close match. Again the experimental current waveform shows a close match in the nature of curve but it is spikier than its counter part in simulation.

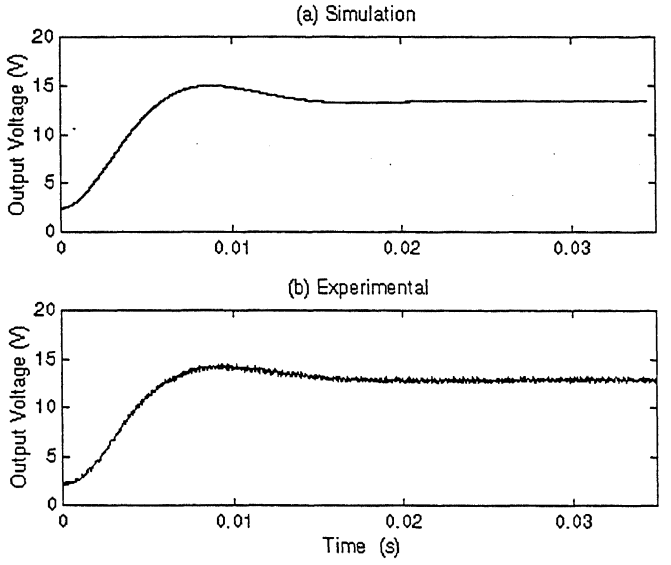


Fig. 2.25 Experimental and simulation result of Output Voltage for $d_0 = 0.2$ and $\tilde{d} = 0.4$

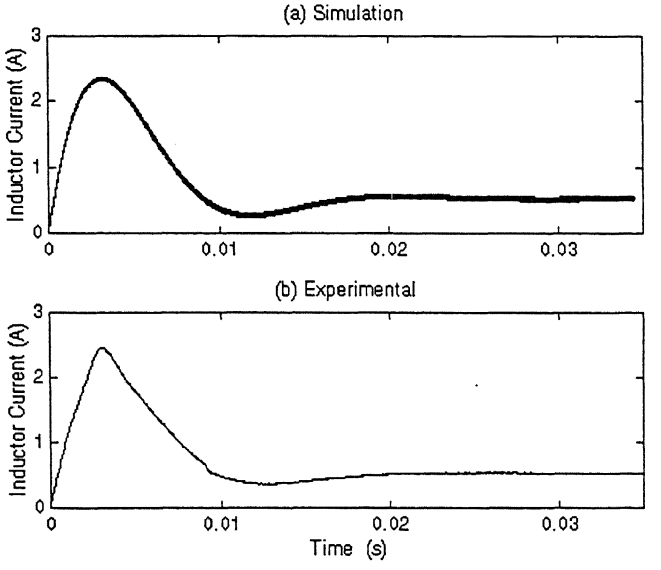


Fig. 2.26 Experimental and simulation result of Inductor Current for $d_0 = 0.2$ and $\tilde{d} = 0.4$

The open loop study for a higher supply voltage (20V) of the converter has also been made. The results are shown in Figs. 2.27 and 2.28. The simulation and experimental results matches closely for the output voltages, however the inductor current indicates the presence

of saturation. It is to be noted that the inductor is subjected to very large current in the transient compared to its steady state nominal current. This does not necessarily require another inductor with larger saturating current, as the controller is capable of regulating the output in presence of saturation. This will be experimentally shown in the next chapter.

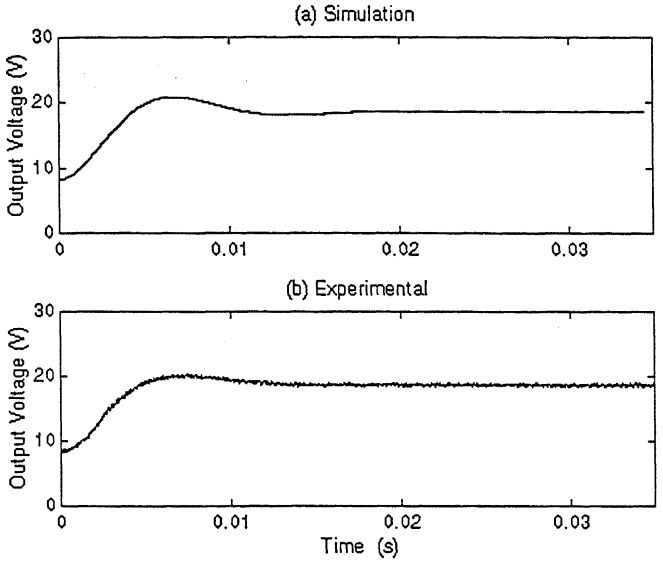


Fig. 2.27 Experimental and simulation result of Output Voltage for $d_0 = 0.3$ and $\tilde{d} = 0.2$

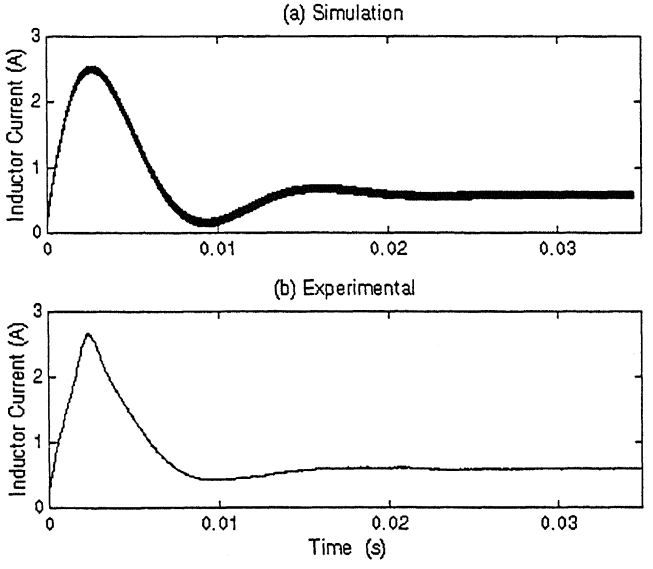


Fig. 2.28 Experimental and simulation result of Inductor Current for $d_0 = 0.3$ and $\tilde{d} = 0.2$

The saturation of the inductor current changes even the profile of the capacitor (output) voltage compared to the ideal simulation. This is clearly seen from Fig. 2.29 where the experimental trace shows an increase in damping of this voltage. The inductor current

obtained through simulation and experimentation do not match during the transient (Fig. 2.30). However, their steady state values are almost same. Thus a controller designed based on the simulated parameters should be able to run even in the presence of the saturation.

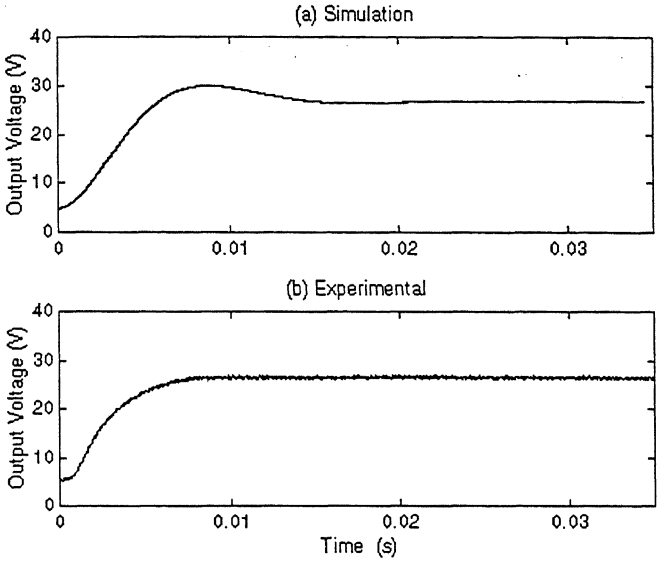


Fig. 2.28 Experimental and simulation result of Output Voltage for $d_0 = 0.2$ and $\tilde{d} = 0.4$

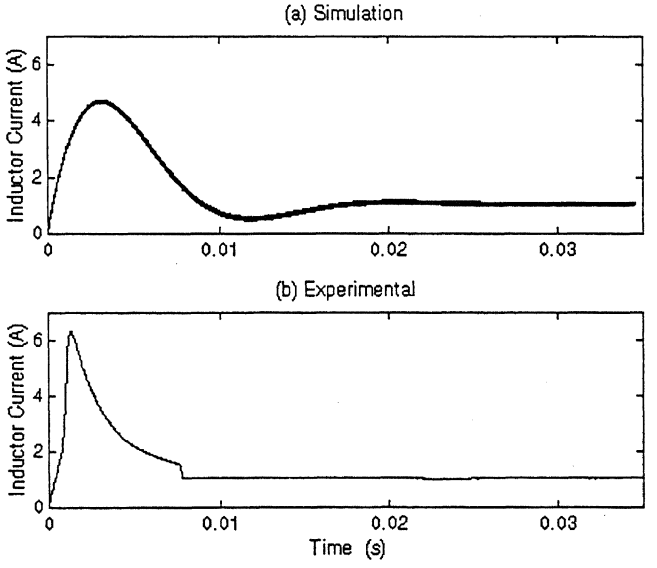


Fig. 2.29 Experimental and simulation result of Inductor Current for $d_0 = 0.2$ and $\tilde{d} = 0.4$

2.7 CONCLUSIONS

In this chapter, novel mathematical models called bilinear corner point prediction model and averaged bilinear prediction model have been derived. These models are verified by extensive simulation studies on a number of DC-DC converters. Experimental verification of simulated system perturbation (SSP) has been carried out for the Buck-Boost converter. This indirectly verifies these models.

It has been observed that bilinear prediction model (BMP) has a better prediction performance compared to other existing models such as linear prediction model (LMP) and state space model (SSA). The bilinear prediction model performs well at reasonably low frequencies and large perturbation in duty ratio. The validity limit of model for perturbation in duty ratio is a function of switching frequency of the converter.

A generalized expression for perturbation of states of a converter with more than two subintervals has been derived. This model helps in modeling converters with more than two subintervals.

CHAPTER 3

CONVENTIONAL BUCK-BOOST CONVERTER: CONTROLLER DESIGN

A DC-DC converter is used for regulated power supply. The regulated power supply must be able to cater to widely varying load and supply conditions. This requires a closed loop control design of the converter. The closed loop converter system must be able to regulate the load and supply disturbances without loosing stability. Ideally the closed loop should account for infinite load and supply disturbances.

The controller parameters are functions of the converter parameter. Therefore better is the converter model, higher is the zone of validity of the controller. In this chapter, different controller design philosophy has been used with linear and bilinear models to determine zone of validity of the closed loop operation. Additionally a fuzzy based multi-zonal controller design to extend the zone of operation of the closed loop system. The converter in this case is modeled by bilinear model in number of small zones in fuzzy domain. It is expected that the converter must be able to cater a still larger set of disturbance in supply and load.

3.1 LINEAR CONTROLLER DESIGN

In this we shall design controller based on the linear model of the converter given in (2.14) and the equation is reproduced below

$$\tilde{x}(k+1) = F\tilde{x}(k) + G\tilde{u}(k) \tag{3.1}$$

$$\tilde{y}(k) = C\tilde{x}(k) \tag{3.2}$$

It is desired that the controller be able to track any step change in the reference voltage $\tilde{y}_{ref}$. Note that $\tilde{y}_{ref}$ is a change in the desired output from the steady state value. For example, if the converter output is 20V in steady state and we want an output of 30V, then the $\tilde{y}_{ref}$ will be 10V. Similarly, if it is desired to have an output voltage of 10V, $\tilde{y}_{ref}$ will be –10V.

To facilitate the tracking function; we include a pseudo-integrator action on the error function $e(k)$ in the feedback loop. This is given by

$$e(k) = \tilde{y}(k) - \tilde{y}_{ref}(k) \tag{3.3}$$

$$z(k+1) = (1-\varepsilon)z(k) + e(k) \tag{3.4}$$

where ε is a very small positive number. We now define an extended state vector as

$$x_e(k) = \begin{bmatrix} \tilde{x}(k) \\ z(k) \end{bmatrix} \tag{3.5}$$

Then combining (3.1) and (3.4) we get an extended state space representation as

$$\begin{aligned} \tilde{x}_e(k+1) &= \begin{bmatrix} F & 0 \\ C & 1-\varepsilon \end{bmatrix} \tilde{x}_e(k) + \begin{bmatrix} G \\ 0 \end{bmatrix} \tilde{u}(k) + \begin{bmatrix} 0 \\ 0 \\ -1 \end{bmatrix} \tilde{y}_{ref}(k) \\ &= F_e\, \tilde{x}_e(k) + G_e \tilde{u}(k) + J_e \tilde{y}_{ref}(k) \end{aligned} \tag{3.6}$$

The output equation thus becomes

$$\begin{aligned} \tilde{y}_{ref}(k) &= \begin{bmatrix} C & 0 \end{bmatrix} \tilde{x}_e(k) \\ &= C_1 \tilde{x}_e(k) \end{aligned} \tag{3.7}$$

Note that the presence of the ε term in the pseudo-integrator can cause steady error. However without this term, the matrix F_I becomes positive semi-definite. The positive definite condition is required for linear quadratic design and also for Lyapunov based design to be discussed later. This pseudo-integrator facilitates control design based on these methods albeit at the cost of minor steady state error.

We now use a linear controller of the form

$$\tilde{u}(k) = -K\tilde{x}_e(k) \tag{3.8}$$

The linear control system block diagram is shown in 3.1. The linear controller is designed based on either pole shifting technique or by linear quadratic regulator. These are discussed below.

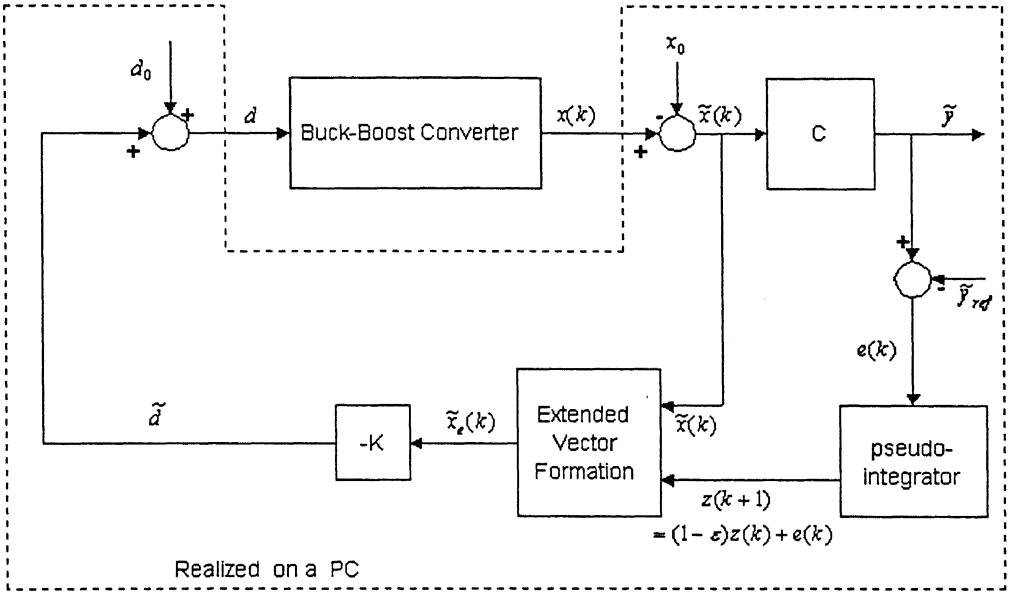


Fig. 3.1 Block diagram of the linear tracking controller

It is to be noted that the closed loop operation of the converter requires nominal duty ratio d_0 to set the value of the reference. The set value may be obtained from the desired output voltage from (2.13) or can be assigned directly.

3.1.1 Pole Placement Controller

To obtain the gain matrix K in (3.8), the pole shift control technique given in [63] is used. In this method, the closed loop poles are obtained by radially shifting the open loop poles to more stable location. The amount $\lambda (0 < \lambda < 1)$ by which the poles are shifted is called the pole shift factor. Consider the open loop poles shown in Fig.

3.2. All the poles can be moved to a more stable location by multiplying the factor λ. The closed loop poles thus generated are $\lambda * eig(F_e)$. The pole shift factor can be viewed as penalty on the control action. When this value is close to 1, a large penalty is applied and the penalty reduces with the reduction in the value of λ. If the penalty is completely removed, a pole shift controller becomes a deadbeat controller for $\lambda=0$, where all the poles are placed at the origin. We can then use the 'place' function of the MATLAB control toolbox to obtain the matrix K or alternatively design this by Ackerman's formula [61]. Below we present the simulation and experimental results with linear pole shift controller.

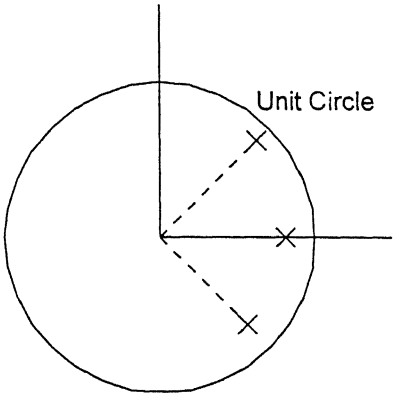


Fig. 3.2 Complex Z plane showing the location of open loop of poles

The simulation and experimental results of each test set is presented on the same graph. Further, the actual output voltage, inductor current and duty ratio are shown on three separate graphs for each test. The test performed and corresponding figure numbers are listed in Table 3.1. The parameters of the Buck-Boost converter chosen for the simulation and experimental verification are:

Inductor: $L = 3mH, R_L = 1.2\Omega$, Capacitor: $C = 330\mu F, esr = 20m\Omega$

Nominal resistance: $R = 64.04\Omega$, Frequency: $F = 26.076\,kHz$

It can be seen from these figures that both simulation and experimental results match closely in most of the cases. The cases in which they are different and the other results are discussed below.

Table 3.1 Summary of the test results with pole shift control

No.	Frequency in KHz	Steady-state Duty Ratio (d_0)	Input Voltage (V_{dc})	Description of the test	Results shown in
1	26	0.3	10	A step change of +10 V in the reference voltage ($\tilde{y}_{ref}$)	Fig. 3.3
2	26	0.3	10	A step change of +15 V in the reference voltage ($\tilde{y}_{ref}$)	Fig. 3.4
3	26	0.7	10	A step change of –5 V in the reference voltage ($\tilde{y}_{ref}$)	Fig. 3.5
4	26	0.3	20	A step change of +20 V in the reference voltage ($\tilde{y}_{ref}$) command	Fig. 3.6
5	26	0.3	20	A step change of +30 V in the reference voltage ($\tilde{y}_{ref}$) command	Fig. 3.7
6	26	0.7	20	A step change of –10 V in the reference voltage ($\tilde{y}_{ref}$) command	Fig. 3.8
7	26	0.3	10	Converter started from a duty ratio 0.01 to attend steady state duty of 0.3	Fig. 3.9
8	26	0.3	10	Converter started from a duty ratio 0.0 to attend steady state duty of 0.3 and load resistance is taken as16 Ω.	Fig. 3.10
9	54	0.3	20	A step change of +25 V in the reference voltage ($\tilde{y}_{ref}$) command	Fig. 3.11

The experimental and simulation waveform for the output voltage, shown in Fig. 3.3(a) matches closely. The inductor current in experimental result has sharper rise compared to the simulation waveform. This may be due to saturation of the inductor. The core due to saturation builds the current rapidly and this results in sharper inductor current waveform. Therefore the duty experiences a short interval dip as shown in the Fig. 3.3(c). Since the saturation of inductance has not been modeled in the simulation programs the simulated waveforms of inductor current and hence the duty ratio does not match the experimental waveforms. The simulation assumes an ideal inductor and therefore shows all smooth graphs for inductor current and duty ratio. The tracking is however perfect in simulation and experiment. It is interesting to note that the graph for all the variables matches perfectly in steady state.

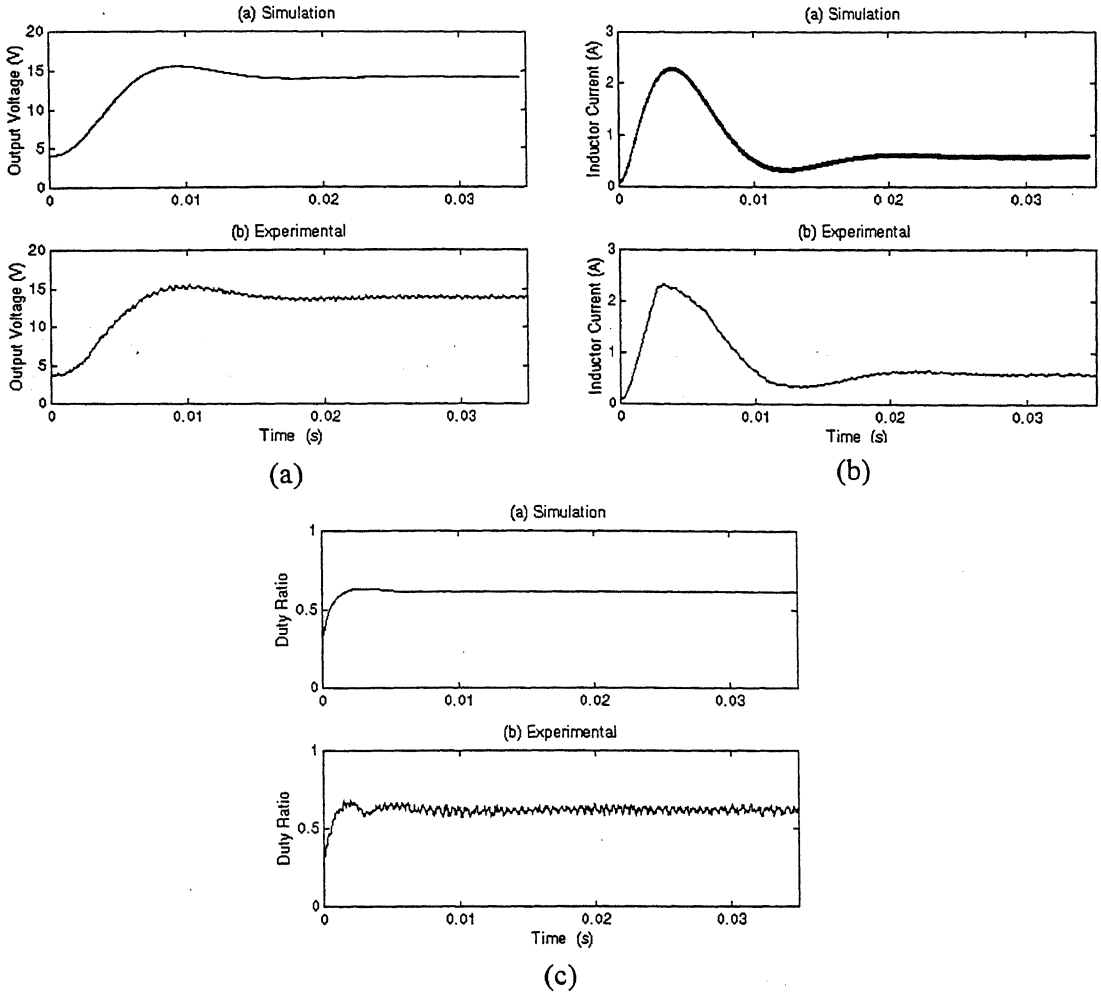


Fig. 3.3 Step change of 10 V when the duty ratio is 0.3

In order to find the tracking limit of the pole shift controller with the linear model of the converter, we have carried out a number of simulation and experiments. Fig. 3.4 shows the result of the test carried out for tracking voltage $\tilde{y}_{ref} = 15V$, when the converter is operating at steady state duty ratio of 0.3, i.e. at a steady state output voltage of 4.1 V. It can be seen from the simulation result that the inductor current has become discontinuous. It is however not discontinuous in experimental result, may be due to the saturation the inductor. The controller although designed for CCM operation, takes in account of the DCM operation for a short interval and the output voltage settles at 19.8 V. It can be seen from Fig. 3.4(c) that the duty ratio has saturated for a very long duration. This means that the controller produces a large control action to track the perturbation in the reference voltage. The controller has been simulated and experimented to track a larger change in the voltage reference than 15V. It has been found that the converter is not able to track larger voltage changes than 15V. The results

are therefore not shown here.

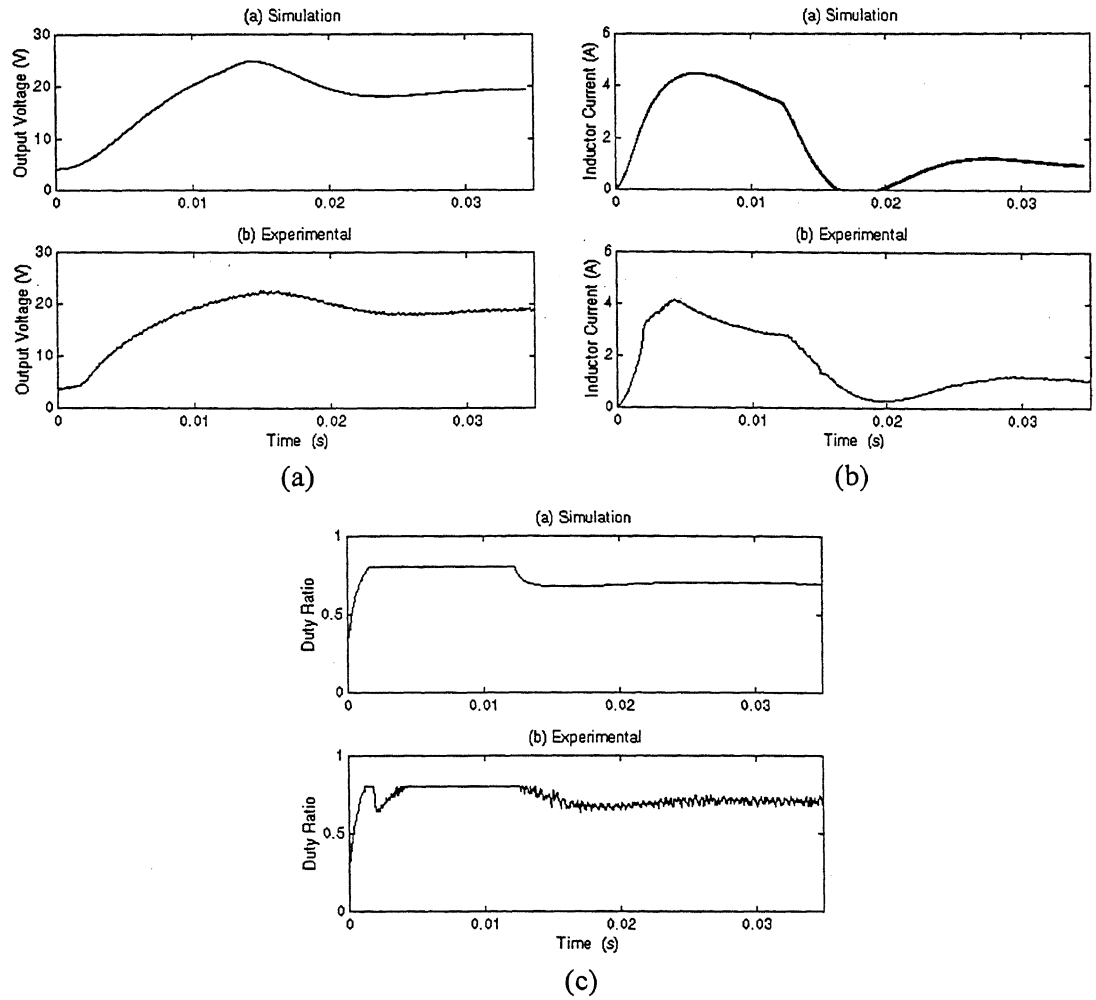


Fig. 3.4 Step change of 15 V when the duty ratio is 0.3

The effect of tracking a negative voltage is presented in Fig. 3.5. The converter is made to operate at steady state duty ratio of 0.7. The steady state voltage at this duty ratio is 18.6 V. It is desired to reduce the steady state voltage by 5V, i.e. $\tilde{y}_{ref} = -5V$.

The test results of simulation and experimentation are shown in Fig. 3.5. It can be seen from the figure that the converter enters into DCM operation during transient. However, the output voltage settles down to the desired output voltage. In order to test for a larger negative tracking, it has been seen that the DCM operation dominated the transient and the controller fails to track a larger voltage.

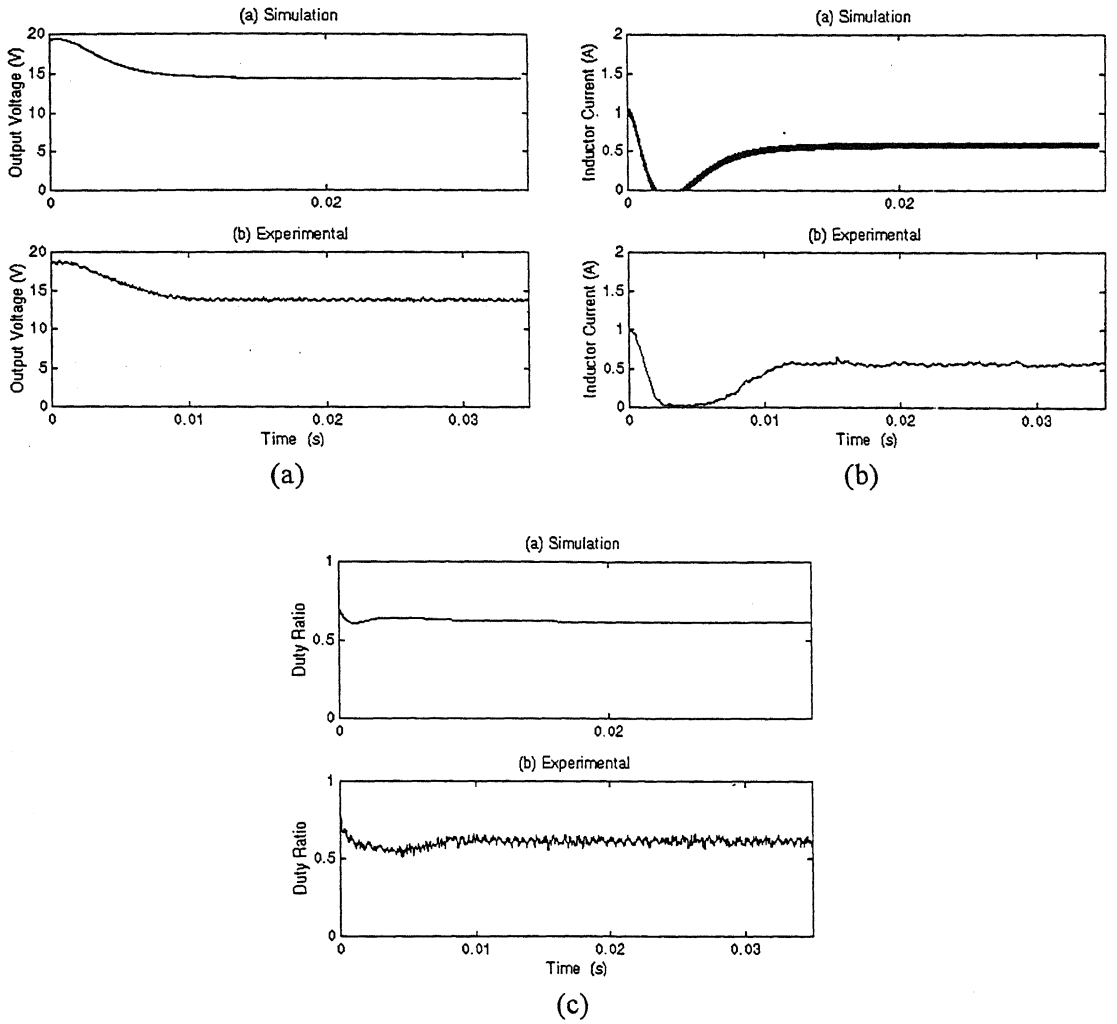


Fig. 3.5 Step change of -5 V when the duty ratio is 0.7

The converter-input voltage is now changed to 20V. The test results are shown in Fig. 3.6 to 3.8. The load resistance is held constant at 64Ω. The converter is made to run at steady state duty ratio of 0.3 for Fig. 3.6 and 3.7. It is desired to track a output voltage change of 20V and 30V respectively. The converter is able to track these changes. However, the effect of saturation is more prominent than previous cases and so is the distortions in the inductor current and duty ratio waveforms shown in Figs. 3.6 and 3.7. In the similar way the test result for tracking a negative voltage of $\tilde{y}_{ref} = -10\,V$ shows DCM operation of the inductor current in Fig. 3.8. In all the cases however, the tracking is limited to 150 % of the supply voltage as it is with $V_{dc} = 10V$. A test for tracking more than 150 % results in instability of the closed loop controller. The closed loop converter is tested at other input voltages also. These results being similar are not repeated here.

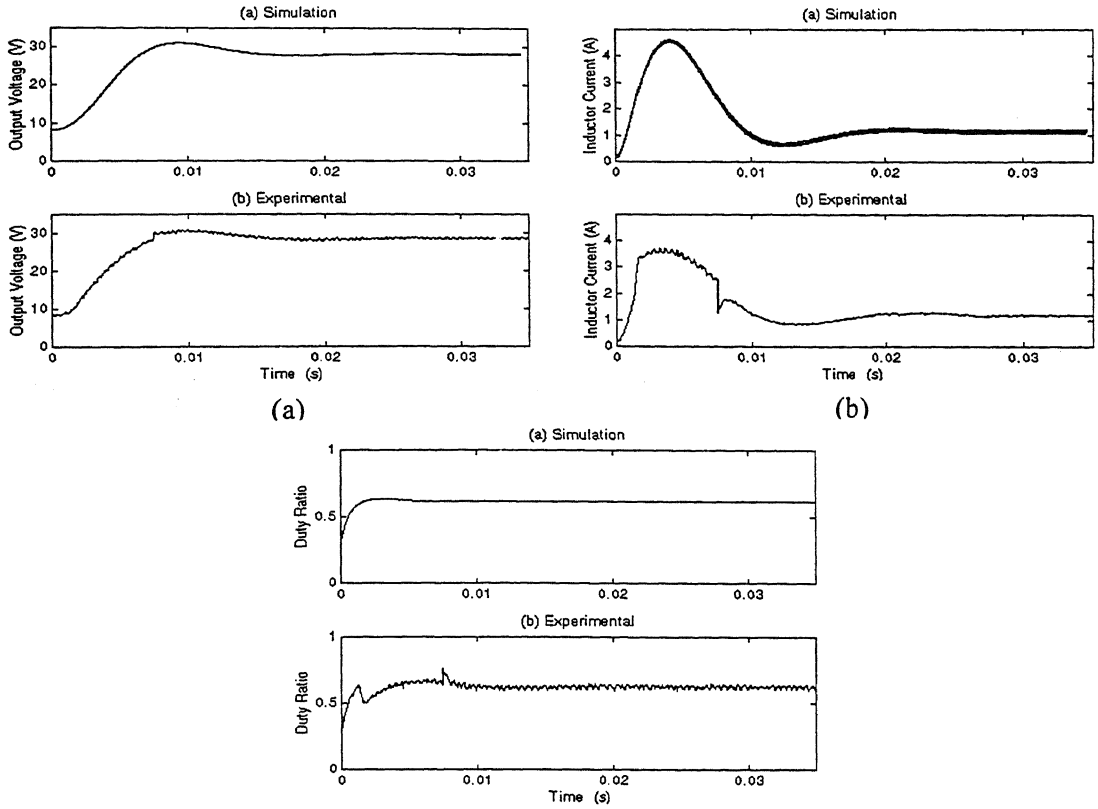


Fig. 3.6 Step change of 20 V when the duty ratio is 0.3

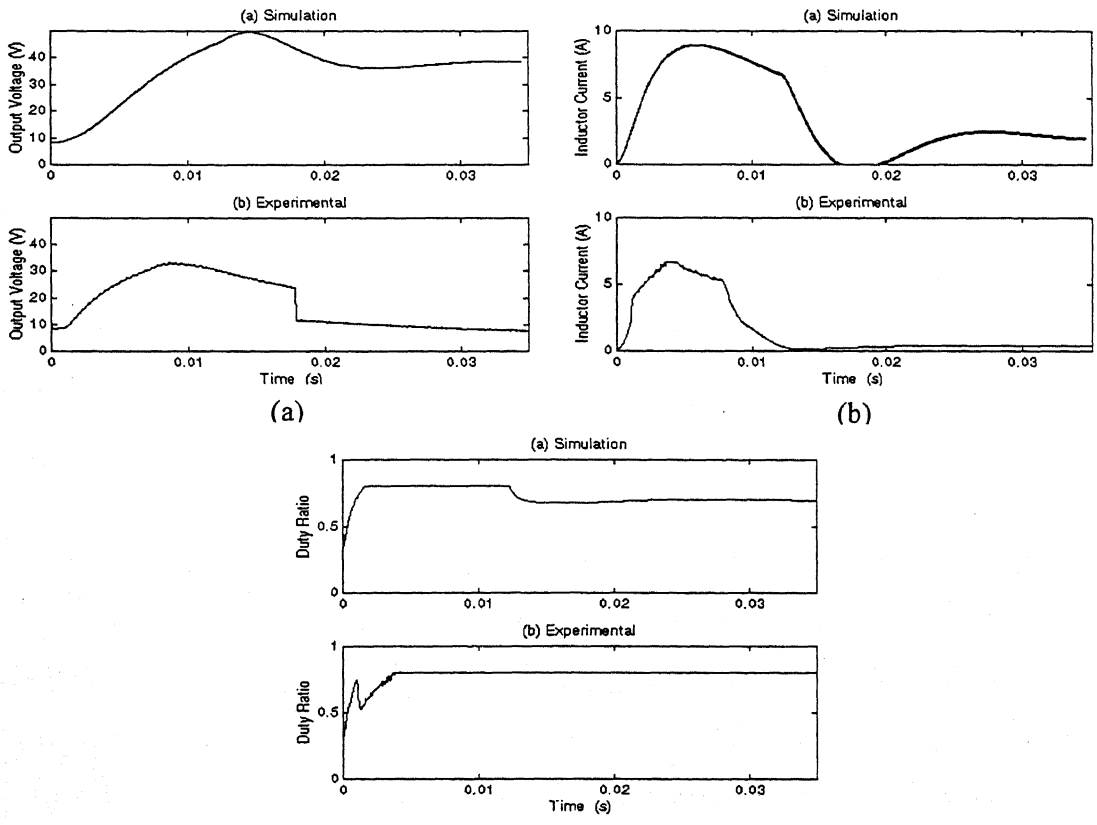


Fig. 3.7 Step change of 30 V when the duty ratio is 0.3

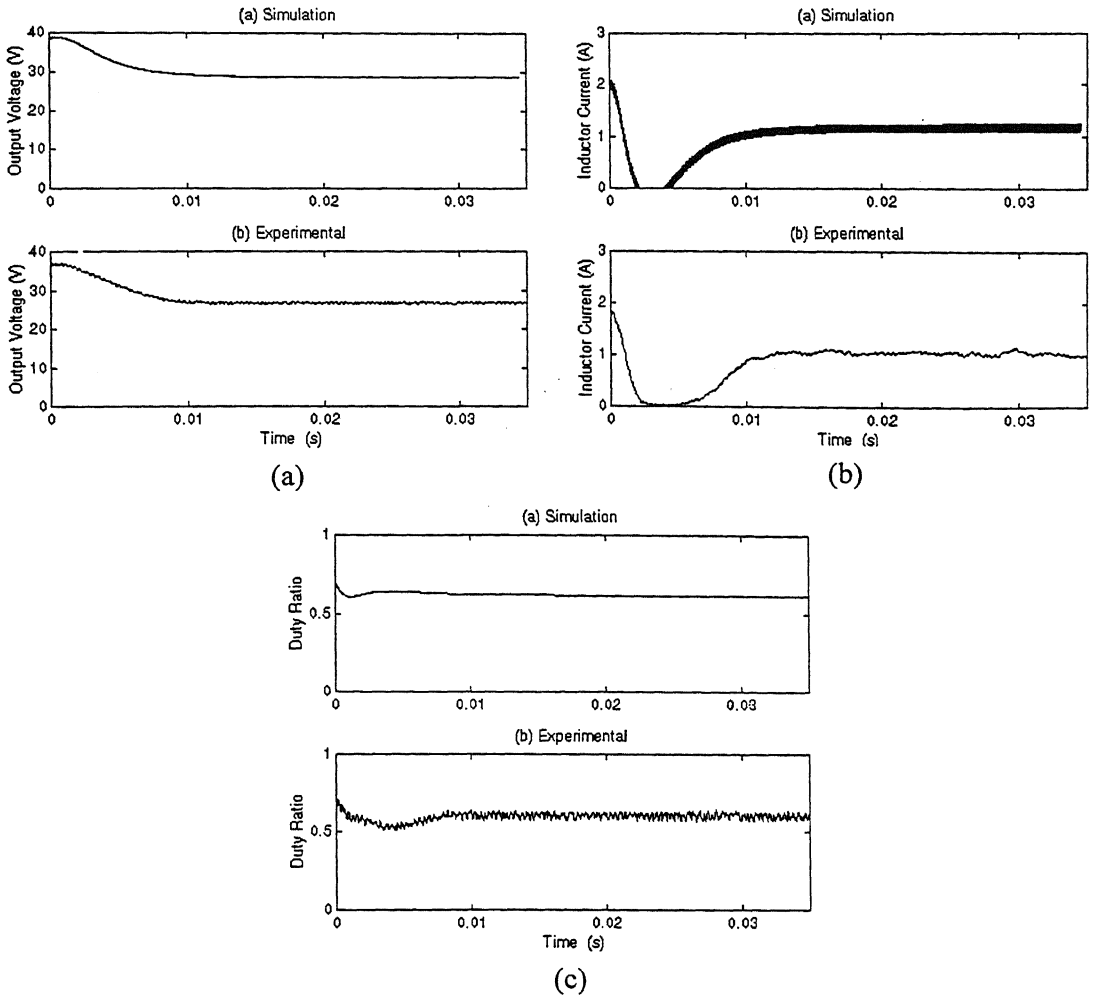


Fig. 3.8 Step change of -10 V when the duty ratio is 0.7

The converter is capable of starting from cold with the closed loop controller designed above for the tracking. The converter is said to be in cold state if its initial conditions are given by

$$\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

The experimental results of cold start of the converter in presence of the controller have been shown in Fig. 3.9. The converter builds up the output voltage smoothly from its cold state. The controller is designed for a load resistance of 64 Ω. Now if we choose a resistance of 16Ω and cold start the converter, the experimental results are as shown in Fig. 3.10. It can be seen from either case that controller can effectively handle cold start. This experiment demonstrates the robustness of the controller.

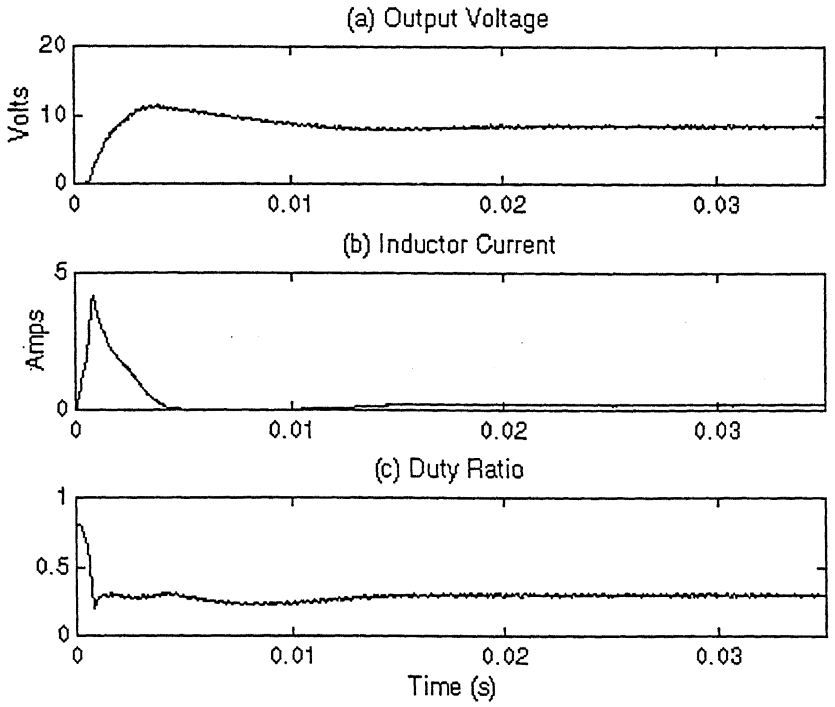


Fig. 3.9 Cold Start behavior with pole placement controller

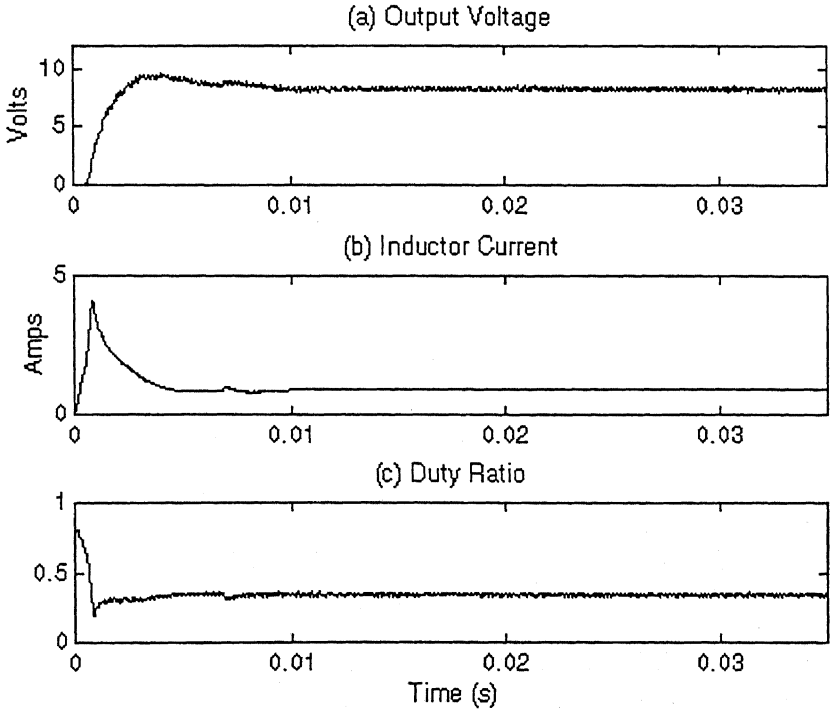
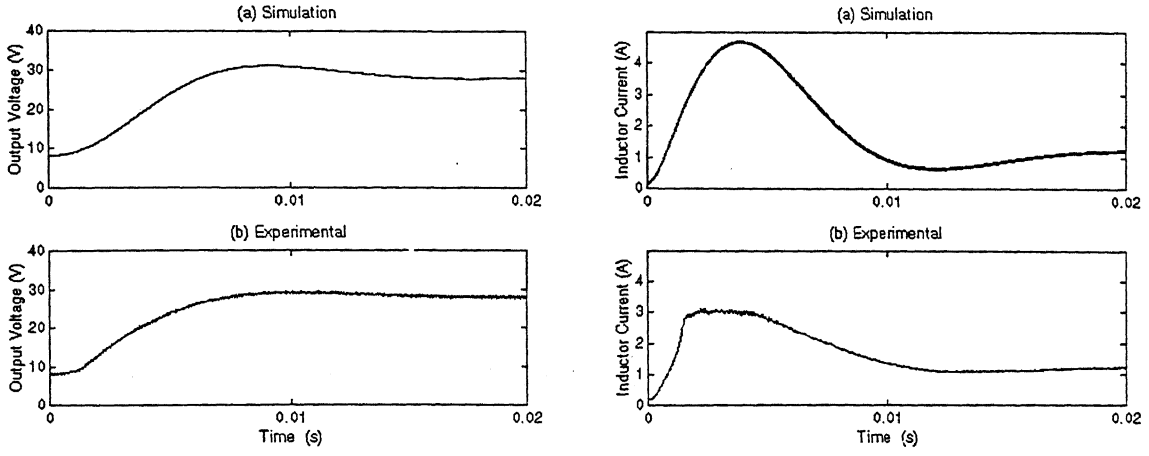
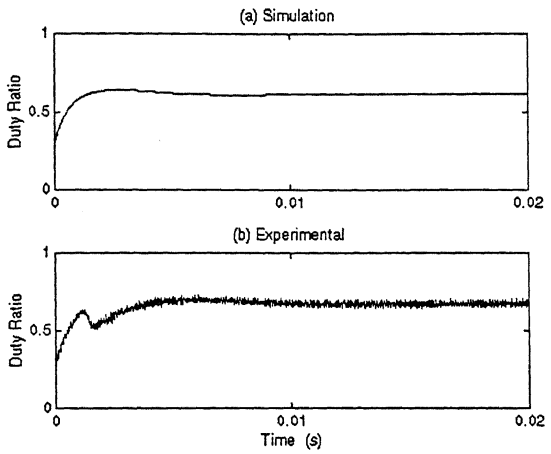


Fig. 3.10 Cold Start behavior with parameters of converter for a different load



(a) (b)



(c)

Fig. 3.11 Step change of 30 V when the duty ratio is 0.3 at 54 kHz

The test carried out in all the previous experiments are at 26KHz. The closed loop converter can however be operated at higher frequencies. To demonstrate the closed loop operation of the converter at a higher frequency, experiment has been carried out at 54 kHz. The test conditions are kept same as to that of the experiment whose results are given in Fig. 3.7. The test results at 54 kHz at these conditions are shown in Fig. 3.11. A comparison of this figure with Fig. 3.7 shows that the closed performance has improved significantly. The inductor current and duty ratio graphs have smoothened. The effect of saturation is less. The higher frequency operation allows faster rate of control action and thus, closed loop operation becomes better compared to its low frequency counterpart. It can thus be said that the operation of the converter at lower frequency can be improved at higher frequencies.

3.1.2 Linear Quadratic Tracking Controller

We choose the extended model given in (3.6) to generate a control of the form (3. 8) through the minimization of the linear quadratic performance index

$$J = \int_0^\infty \left(\tilde{x}_e^t Q \tilde{x}_e + \tilde{u}(k) \Re \tilde{u}(k) \right) dt \tag{3.9}$$

In this Q is a positive definite matrix of dimension 3x3 and $\Re$ is positive scalar penalty on the control. Due to weighting and penalization of state and control input, it is expected that stability margin will increase and the control action will be smoother compared to pole placement controller. The block diagram of the closed loop system with linear quadratic based controller is the same as that shown in Fig. 3.1 except that the gains are computed off line through matrix Riccati equation.

The value of penalty on control $\Re$ is chosen to be a very large quantity in order to restrict the control effort leading to saturation of the duty ratio. The weighting of the states has been taken to be a very small quantity and is equal to $0.002\,[I]_{3x3}$. The value of the penalty on control is 100000 in simulation and experiment. The said value of the penalty on control has been obtained from extensive simulation study for a better dynamic response. The control action is obtained by optimization of cost function J. MATLAB function LQR has been used to obtain the gain matrix K. We now use this gain matrix for the simulation and experimentation. The experimental and simulation results are shown in Fig. 3.12 to 3.14. Fig. 3.12 shows the tracking performance of the closed loop controller for $\tilde{y}_{ref} = 20V$ at $V_{dc} = 20V$. The maximum tracking capability of this controller is 35 V which is 150 % of the supply voltage. Thus, the maximum tracking capability remaining unchanged as compared to the pole placement controller. However, the duty ratio becomes smoother.

The performance of the controller has been tested for cold starting with rated loading of 64 Ω (Fig. 3.13) and with changed loading of 16Ω (Fig. 3.14). The performance is better than with pole shift controller. It can be seen that the duty ratio with this control almost attains steady state value as soon as the converter is switched on. This is unlike the previous case with pole shift controller where the transient in duty ratio is noticeable.

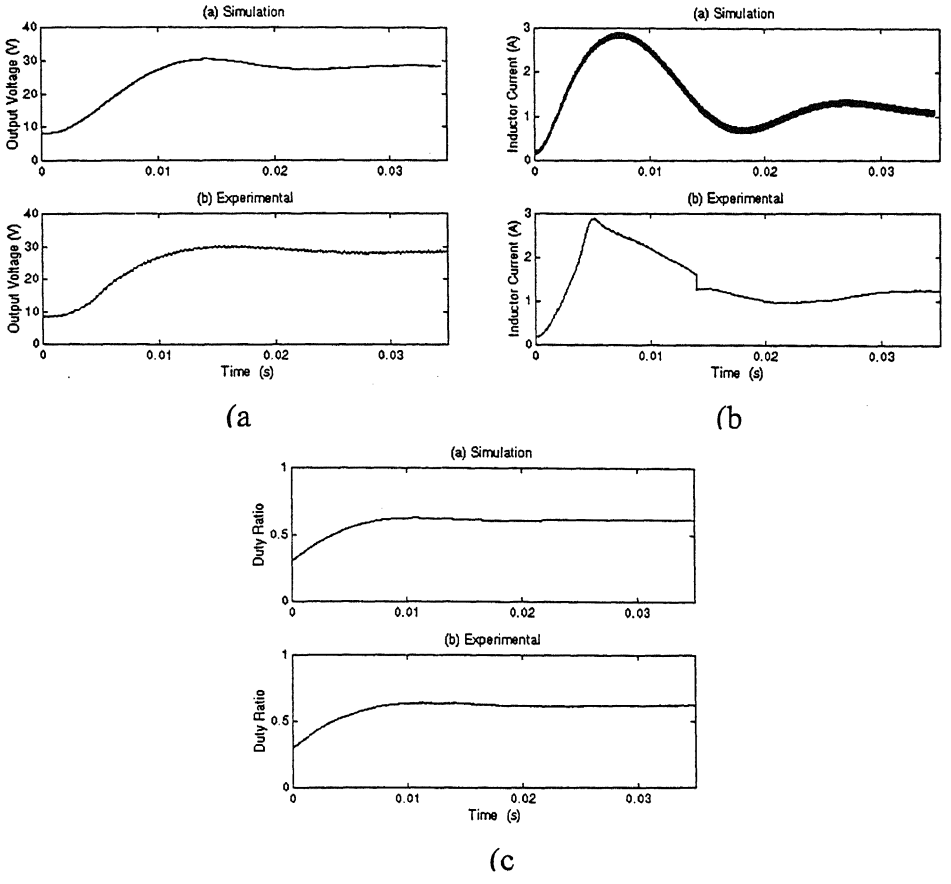


Fig. 3.12 Step change of 20 V when the duty ratio is 0.3 at 54 kHz

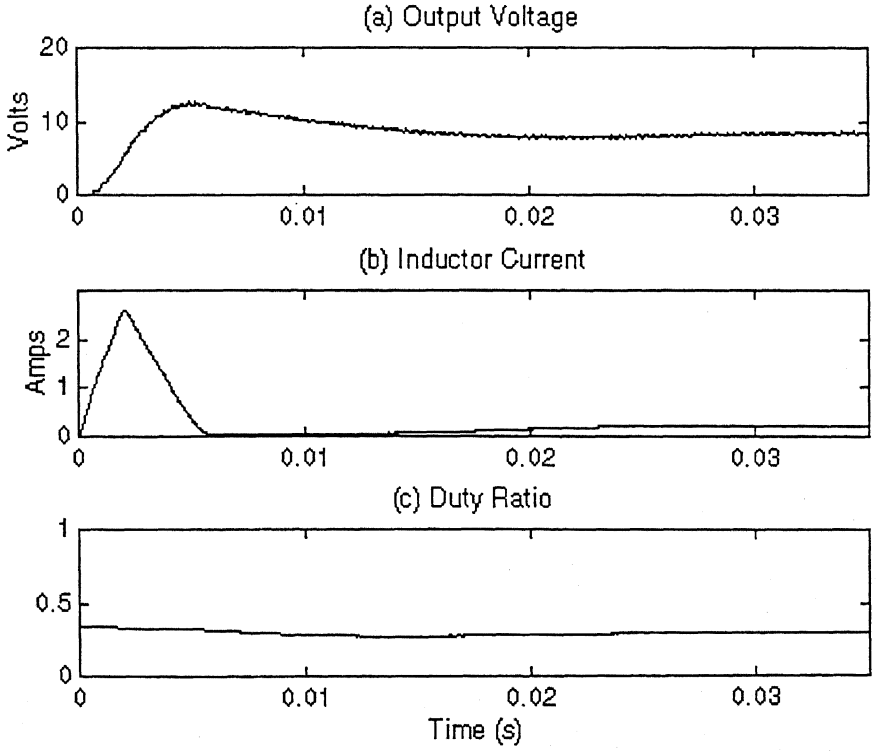


Fig. 3.13 Cold start behavior with LQR controller

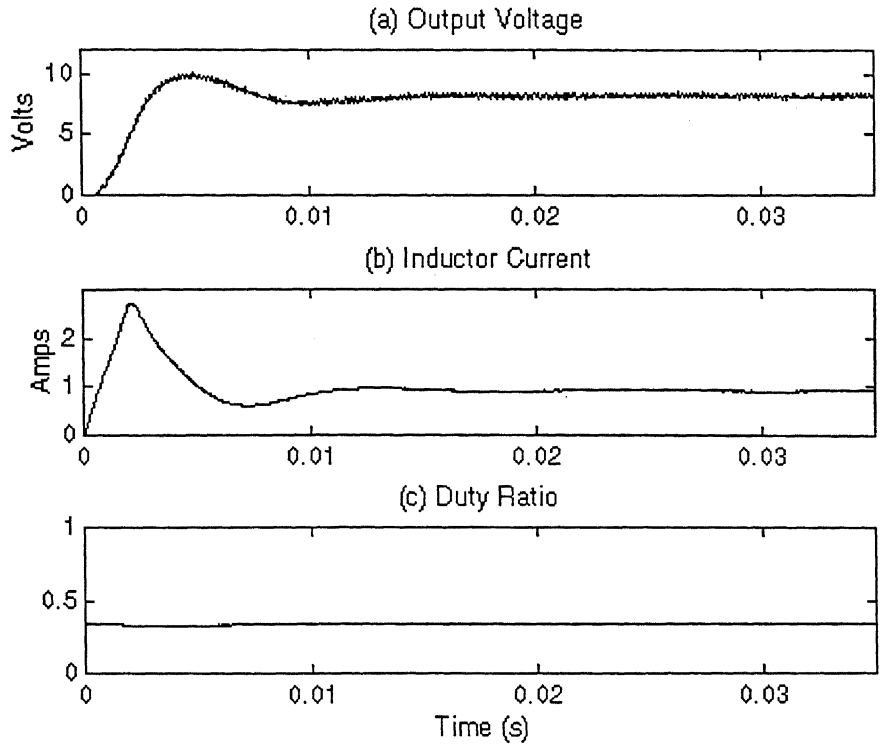


Fig. 3.14 Cold starting of closed loop converter with LQR controller and load of 16Ω

3.2 CONTROLLER BASED ON BILINEAR MODEL

The bilinear model of the converter has less modeling error compared to linear model as shown in Chapter 2. The bilinear converter model given by (2.19) is rewritten below

$$\tilde{x}(k+1) = F\tilde{x}(k) + G\tilde{d}(k) + H\tilde{x}(k)\tilde{d}(k)$$

or,
$$\tilde{x}(k+1) = F\tilde{x}(k) + G\tilde{u}(k) + H\tilde{x}(k)\tilde{u}(k) \tag{3.10}$$

Based on the above model we can derive two control laws. One is with a pseudo-integrator as given in section 3.1 and another with a pure integrator to be discussed in here in subsection 3.2.2. Both of them use Lyapunov stability theorem.

3.2.1 Controller with Pseudo-integrator

Combining (3.4), (3.5) and (3.10), we get an extended state space model of the form

$$\tilde{x}_e(k+1) = \begin{bmatrix} F & 0 \\ C & 1-\varepsilon \end{bmatrix}\tilde{x}_e(k) + \begin{bmatrix} G \\ 0 \end{bmatrix}\tilde{u}(k) + \begin{bmatrix} H & 0 \\ 0 & 0 \end{bmatrix}\tilde{x}_e(k)\tilde{u}(k) + \begin{bmatrix} 0 \\ 0 \\ -1 \end{bmatrix}\tilde{y}_{ref}(k)$$

$$= F_e\tilde{x}_e(k) + G_e\tilde{u}(k) + H_e\tilde{x}_e(k)\tilde{u}(k) + J_1\tilde{y}_{ref}(k) \tag{3.11}$$

We now choose Lyapunov function candidate

$$V(k) = \tilde{x}_e^t(k) P \tilde{x}_e(k) \tag{3.12}$$

where P is a positive definite matrix. The closed loop system will be stable if the following relation is valid

$$\Delta V(k) = V(k+1) - V(k) < 0 \tag{3.13}$$

The control that achieves this is given by

$$\tilde{u}(k) = \frac{-\tilde{x}_e^T(k) F_e^T P\left(G_e + H_e \tilde{x}_e(k)\right) - \left[G_e^T + \tilde{x}_e^T(k) H_e^T\right] P J_e(k) \tilde{y}_{ref}(k)}{G_e^T P G_e + \tilde{x}_e^T(k) H_e^T \left[2G_e + H_e \tilde{x}_e(k)\right]} \tag{3.14}$$

The detailed derivation is given in Appendix B.1.

The experimental and simulation results of closed loop converter are presented below in Fig. 3.15 to 3.19 for different operating conditions. The dummy factor ε for the pseudo-controller is taken to be $1e-5$. The supply voltage and load resistance is respectively 20V and 64 Ω

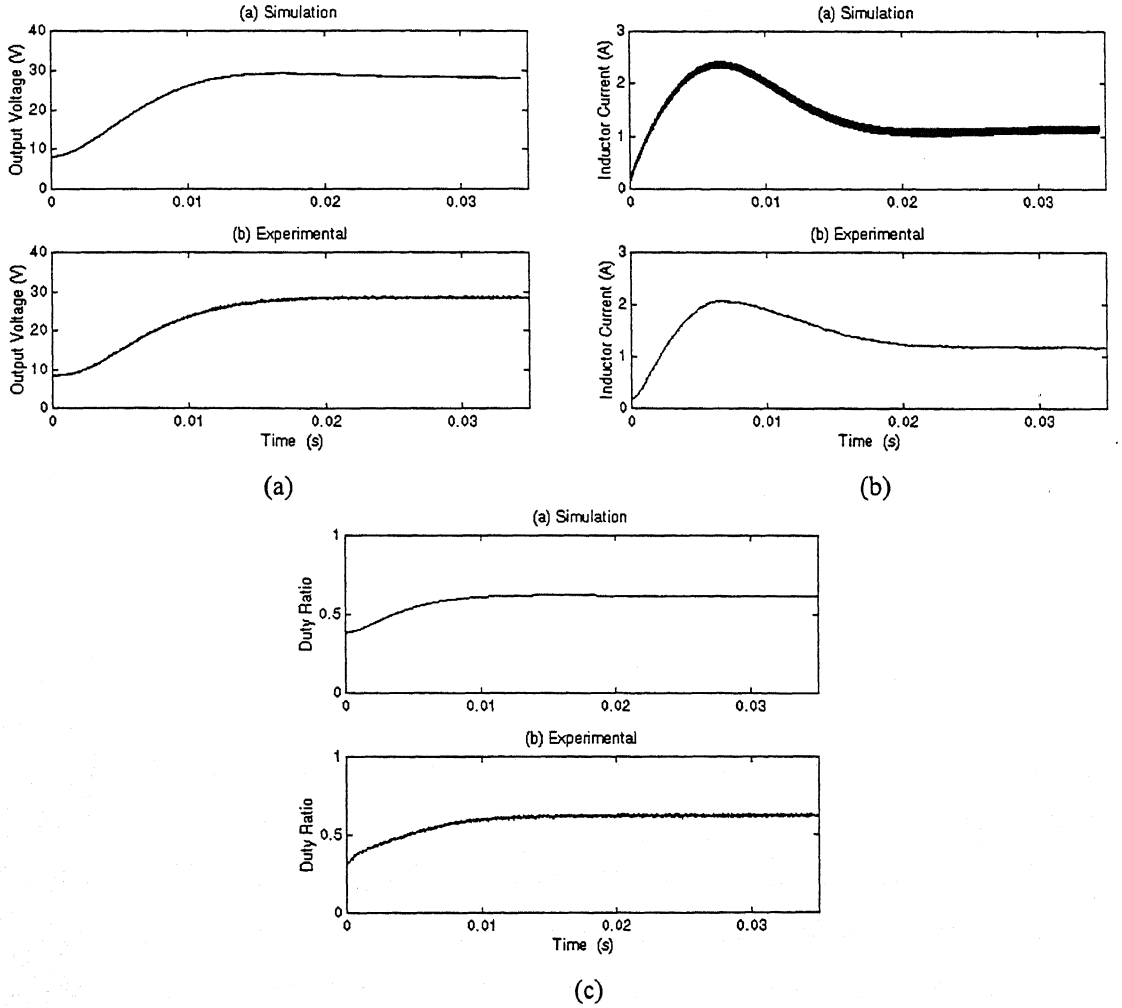


Fig. 3.15 Step change of 20 V when the duty ratio is 0.3

It can be seen from Fig. 3.15 and 3.16 that the control action is smoother than LQR based controller of Fig. 3.12. Furthermore, the controller is capable of tracking higher step voltage command compared to LQR or pole placement controllers since it can successfully track a step change of 30V. The experimental waveforms have slight variation from the simulation results due to saturation in the inductor current. Maximum tracking possible with this controller is 35 V, which 175 % of the supply voltage. Fig. 3.16 shows voltage, current and duty ratio waveform when the change in reference is of 30V.

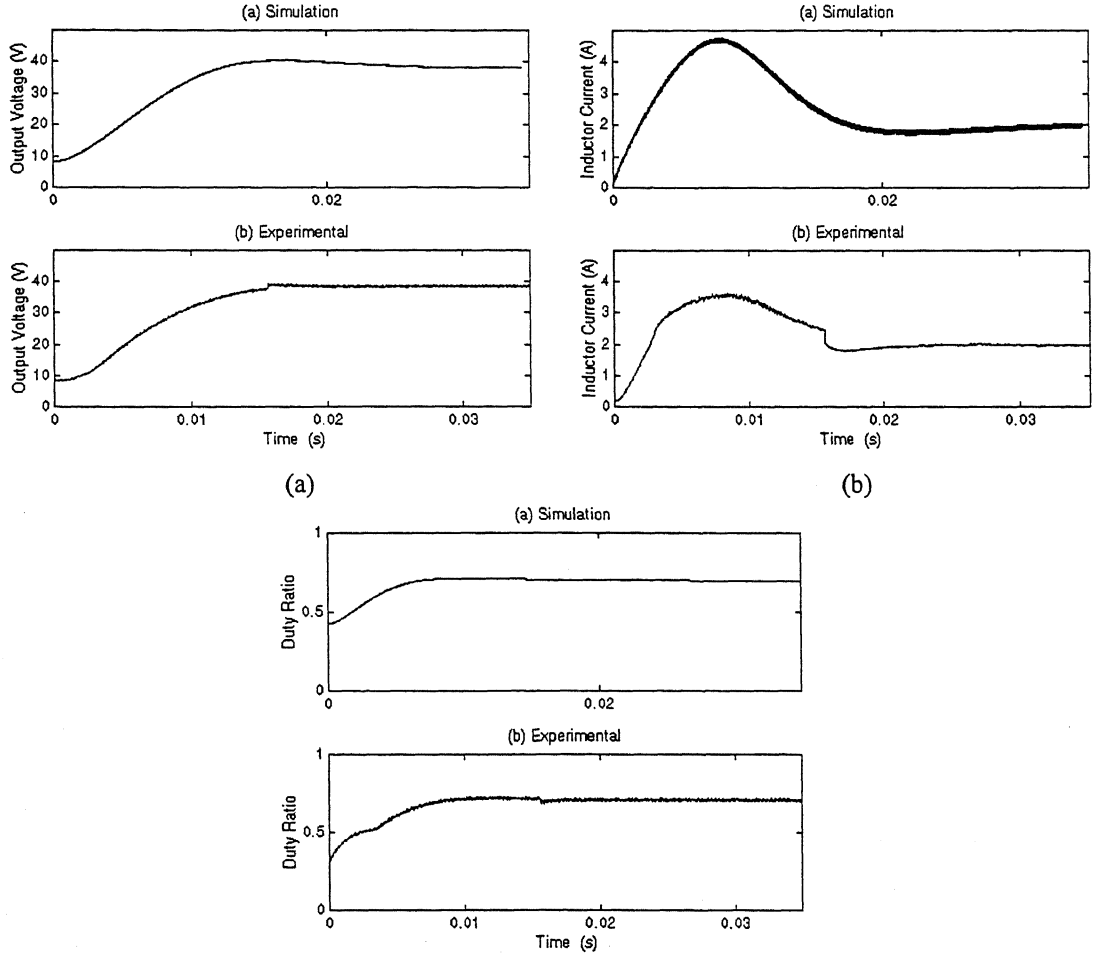


Fig. 3.16 Step change of 30 V wh duty ratio is 0.3 and $V_{dc} = 20V$

The simulation and experimental results for tracking command of 40V is shown in Fig. 3.17. It can be seen that the closed loop system response is unstable in both simulation and experiment. The control input hits the saturation level and stays there forever shown in Fig. 3.17(c). The converter is however able to track 35V reference command, the results are not shown here. This shows an increase by 15V compared to the LQR based

closed loop controller performance. Further the control action is smoother compared to controller based on the linear converter models.

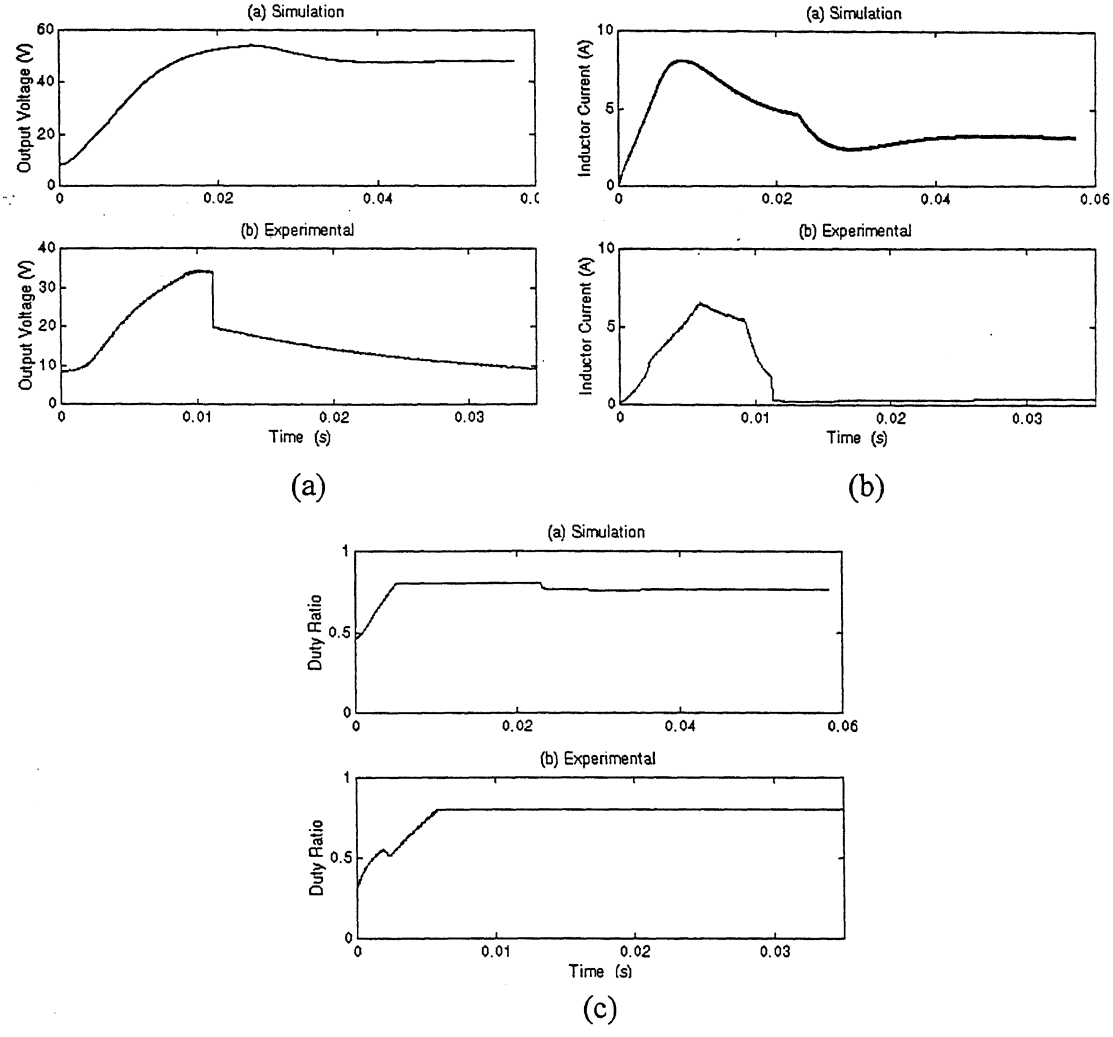


Fig. 3.17 Step change of 40 V when the duty ratio is 0.3

The closed loop converter system is tested for cold start condition. The experimental results are given in Fig. 3.18 and 3.19. The test result shown in Fig. 3.19 is closed loop performance when the converter is started from cold at rated load with controller. The control action is smooth as system settles gradually.

The test result shown in Fig. 3.19 for cold with a load of 16Ω when the controller is design with a load of 64 Ω. The closed loop takes in account of the resistance change and able to track the reference voltage. This proves that the control system is robust.

It is to be noted that the controller based on linear model also have the similar

characteristics in cold start conditions, but the smoothness of the control effort is better in present case compared to previous cases.

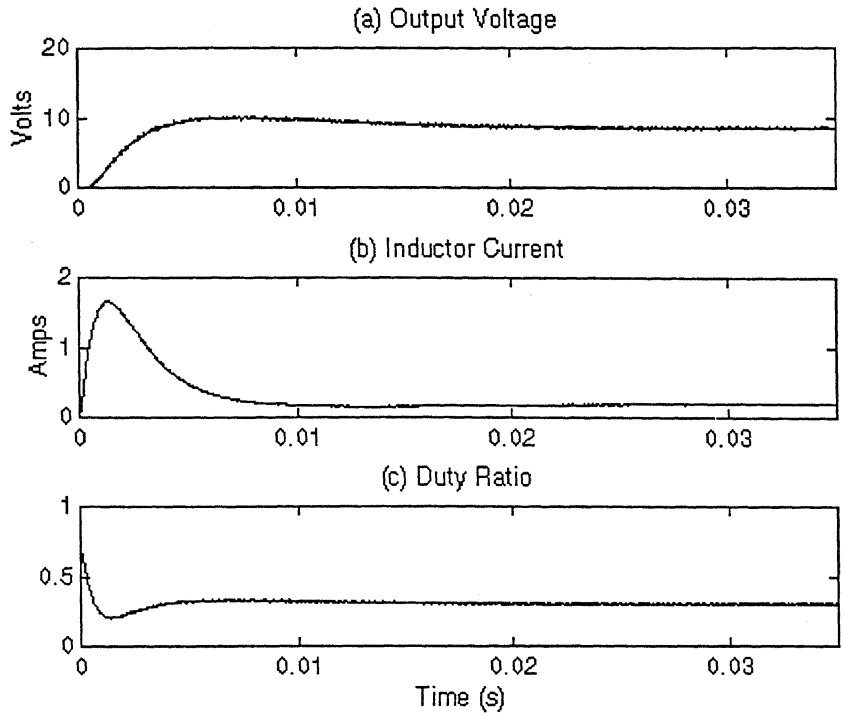


Fig. 3.18 Experimental results of cold starting with bilinear model based controller

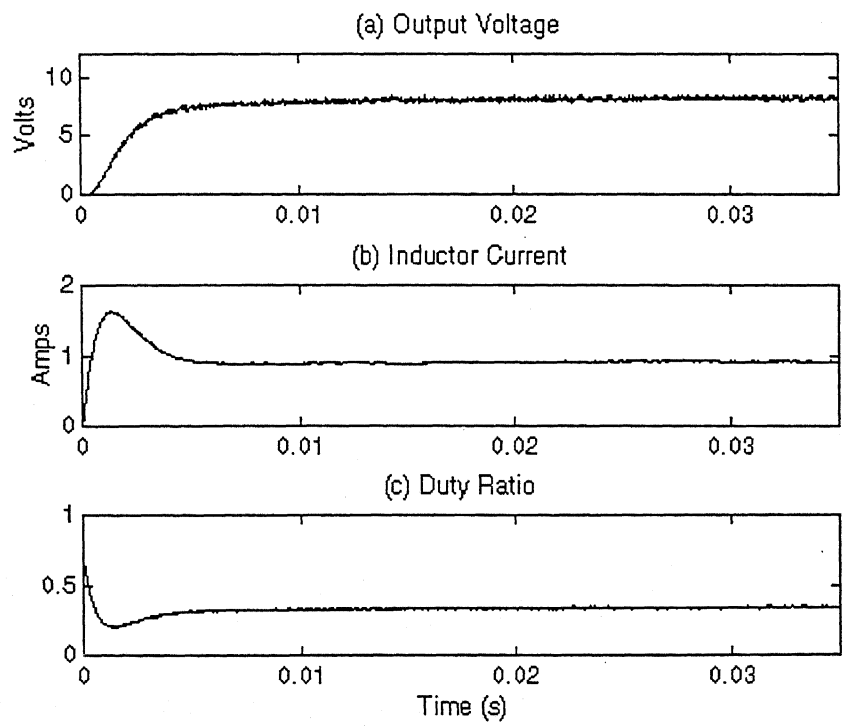


Fig. 3.19 Experimental results for cold starting with perturbed load resistance

3.2.2 Controller with Pure-integrator

The controller given in the previous subsection uses a pseudo-integrator and that can lead to steady state errors. The rationale behind using a pseudo-integrator rather than a pure integrator is that this makes all the eigenvalues of F_e lie inside the unite circle. With the pure integrator one eigenvalues that is associated with integral controller mode will be on unity circle. For this case, we have to make suitable modification to state equation.

Let the integral controller be given by

$$z(k) = z(k) + K_i\, e(k) \tag{3.15}$$

Where K_i is the integral gain. Now for the extended state equation of (3.5), combining (3.10) with (3.15) we get

$$\tilde{x}_e(k+1) = \begin{bmatrix} F & 0 \\ K_i C & 1 \end{bmatrix} \tilde{x}_e(k) + \begin{bmatrix} G \\ 0 \end{bmatrix} \tilde{u}(k) + \begin{bmatrix} H & 0 \\ 0 & 0 \end{bmatrix} \tilde{x}_e(k)\tilde{u}(k) + \begin{bmatrix} 0 \\ 0 \\ -K_i \end{bmatrix} \tilde{y}_{ref}(k)$$

or $$\tilde{x}_e(k+1) = F_1 \tilde{x}_e(k) + G_1 \tilde{u}(k) + H_1 \tilde{x}_e(k)\tilde{u}(k) + J_1 \tilde{y}_{ref}(k) \tag{3.16}$$

Let the control input $\tilde{u}(k)$ is given by

$$\tilde{u}(k) = -L\tilde{x}_e(k) + v(k) \tag{3.17}$$

Where L is a row vector and v(k) is an augmented input. Substituting (3.17) into (3.16) gives

$$\tilde{x}_e(k+1) = F_e \tilde{x}_e(k) + G_e v(k) + H_e \tilde{x}_e(k) v(k) - H_1 \tilde{x}_e(k) L \tilde{x}_e(k) + J_1 \tilde{y}_{ref}(k) \tag{3.18}$$

where $$F_e = (F_1 - G_1 L)\,;\, G_e = G_1\,;\, H_e = H_1 \tag{3.19}$$

We shall now use the Lyapunov function candidate given in (3.12) and design a controller such that (3.13) remains valid. The controller is derived in Appendix C.2, is given by

$$v(k) = \frac{-x_e^T(k) F_e^T P\left(G_e + H_e x_e(k)\right) - \left[G_e^T + x_e^T(k) H_e^T\right] P w(k)}{G_e^T P G_e + x_e^T(k) H_e^T \left[2G_e + H_e x_e(k)\right]} \tag{3.20}$$

where $w(k) = \left[J_e \tilde{y}_{ref}(k) - H_1 \tilde{x}_e(k) L \tilde{x}_e(k)\right]$

The block diagram of the closed loop system is given in Fig. 3.20. It is to be noted from equation (3.20) that the control law is more computationally extensive as compared to the control law based on the pseudo-integral due the presence of matrix product $L_1 x_e$ and term $w(k)$. The simulation results of pseudo-integral based controller presented in last subsection 3.2.1 and the simulation results of pure integral based controller presented below are comparable. Therefore, for practical purposes, the pseudo-integral based controller is better than pure integral based controller because it requires less computation. The control law derived in (3.20) is therefore verified by simulation studies only.

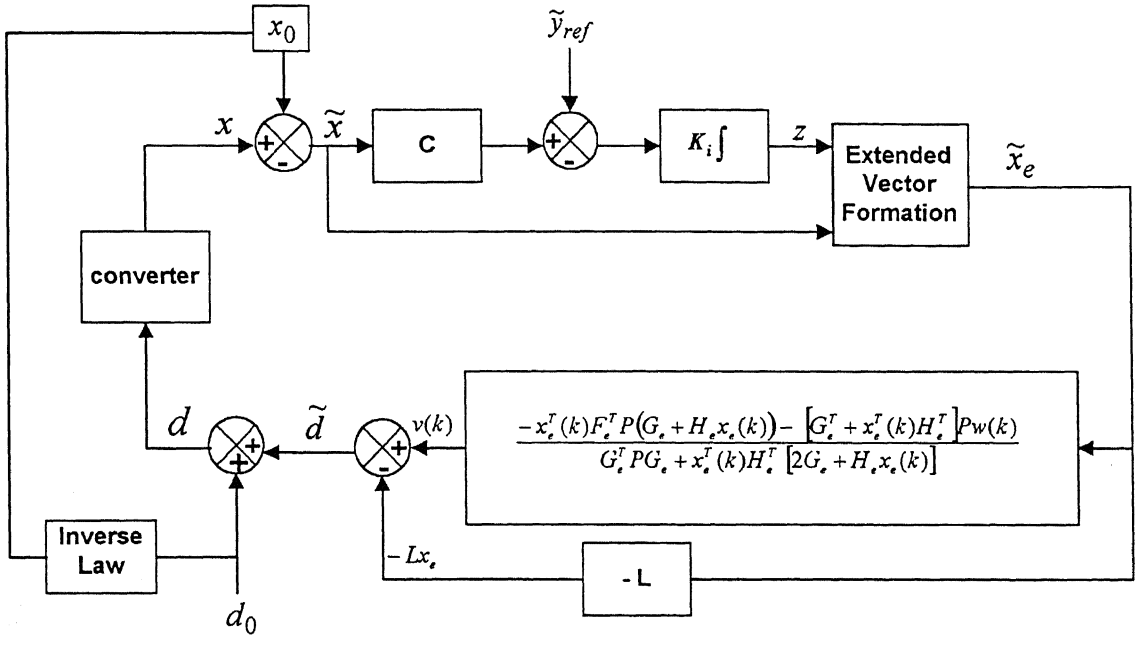


Fig.3.20 Block diagram of closed loop controller based on Pure Integrator

The poles in the simulation studies given below uses pole shift factor of $\lambda = 0.95$, whereas the integral gain is $K_i = 5 * 10^{-5}$. The supply voltage and load resistance is respectively 20V and 64 Ω. The converter is operated at a frequency of 26 kHz. The closed loop system has been simulated for various tracking voltages and the results are given in Fig. 3.21 to Fig. 3.23.

It can be seen from the simulation results that while tracking 30 V change in the reference the duty ratio in Fig. 3.22 is saturating in transient whereas the duty ratio in Fig. 3.16 is not saturating. A proper choice of integral gain and pole shift factor can match these results. The results shown in Fig. 3.17 and Fig. 3.23 are identical in nature.

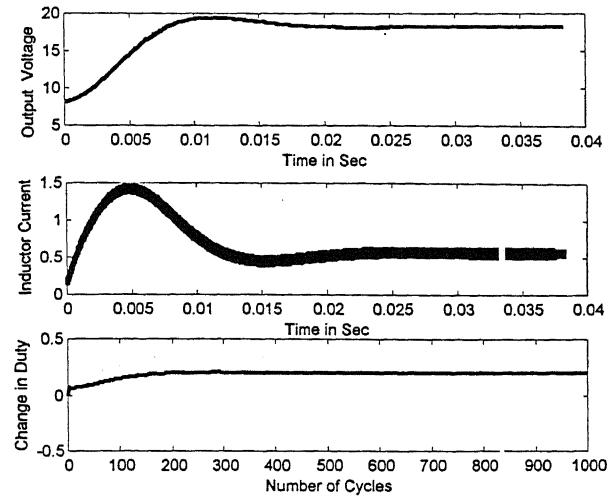


Fig. 3.21 Reference change of 10V with bilinear model based pure integrator Controller

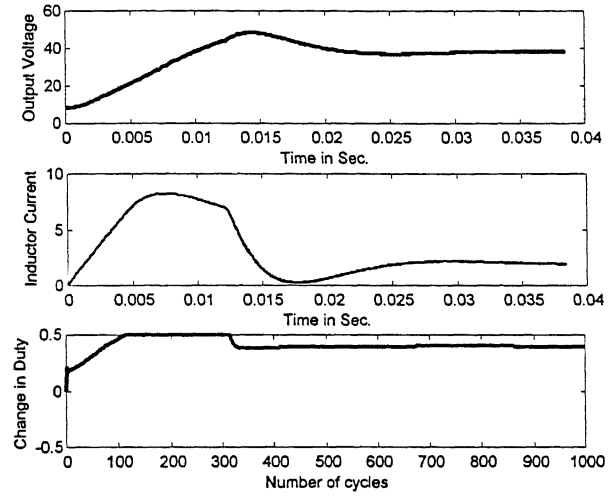


Fig. 3.22 Reference change of 30V with Bilinear model based pure integrator Controller

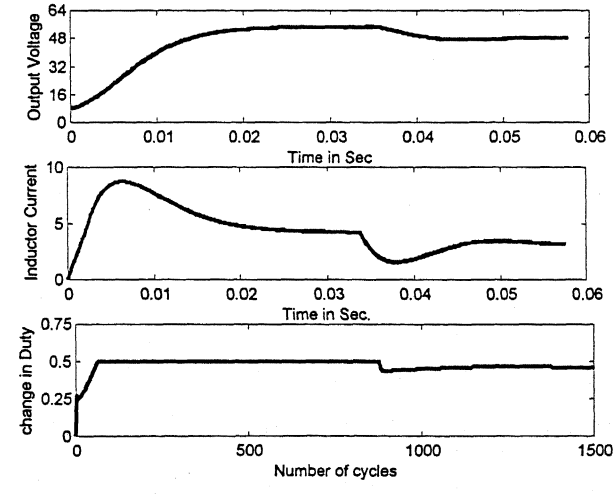


Fig. 3.23 Reference change of 40V with Bilinear model based pure integrator Controller

3.3 MISCELLANEOUS OPERATING CONDITIONS AND THEIR SIMULATION STUDY

A number of load and supply disturbances can occur in a practical system. It is difficult to verify all of them experimentally and thus simulation study of these conditions has been carried out in this section. Since simulation result matches closely to experimental results in almost all the previous cases described in section 3.1 and 3.2, it can be presumed that the simulation results obtained in this section will also have close match with the experimental results.

With the reference command $\tilde{y}_{ref}$ remaining zero, the supply voltage increased by 10 V when the converter was operating with $V_{dc} = 20\,V$ and duty ratio of 0.3. The closed loop is regulated by LQR controller. The results are shown in Fig. 3.24. It is able to stabilize against perturbation in the supply, but requires a very large time to settle down. Further, the converter goes into the DCM mode in the transient.

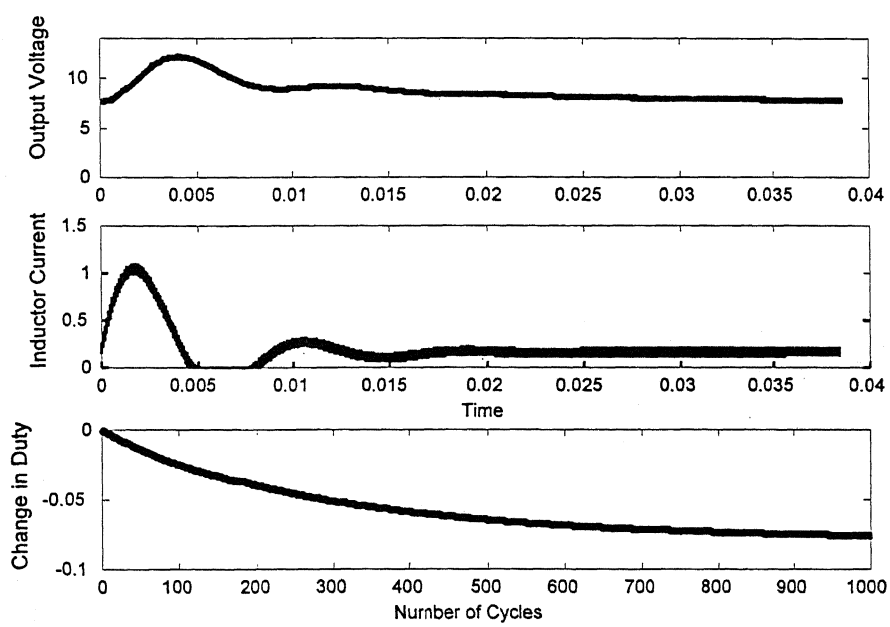


Fig. 3.24 Effect of supply voltage change with LQR Controller

The performance of the bilinear model based controller is shown in Fig. 3.25. The converter never goes into DCM. The peak overshoot is small and duty ratio after an initial transient settles down smoothly. The settling time for both the closed loop systems are approximately 0.02 seconds.

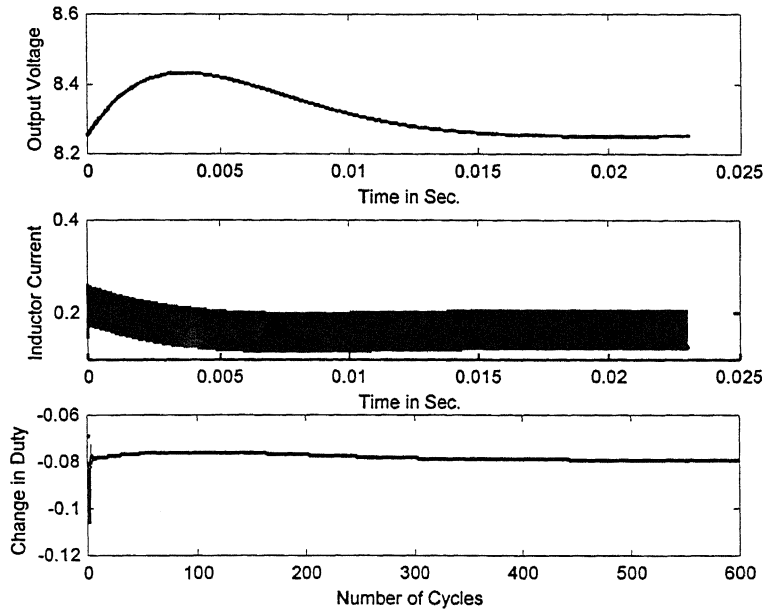


Fig. 3.25 Effect of supply voltage change with Lyapunov Controller

The load resistance is changed to 164 Ω at $t = 0$. The controller is tuned at 64 Ω. The simulation results are shown in Fig. 3.26. It is clear from the figure that the controller is able to reject the load disturbance. Due to light loading, the converter has a small interval of DCM in transient and large ripple in inductor current in steady state.

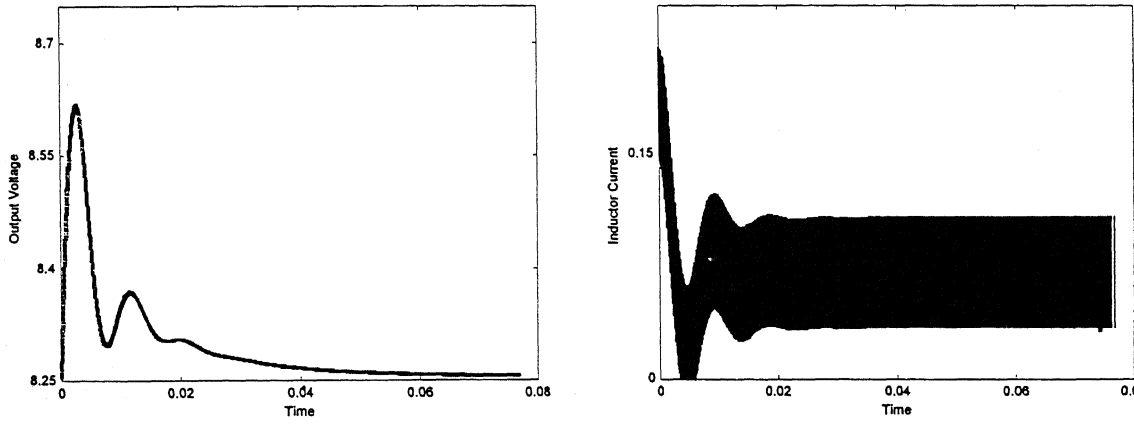


Fig. 3.26 Effect of load variation on closed loop response with LQR Controller

The simulation results for these conditions with bilinear-based controller are shown in Fig. 3.27. It can be easily figured out from comparison of Figs. 3.26 and Fig. 3.27 that the bilinear model based controller performs better. The settling time of LQR and bilinear model based controller are approximately 0.06 seconds and 0.02 respectively.

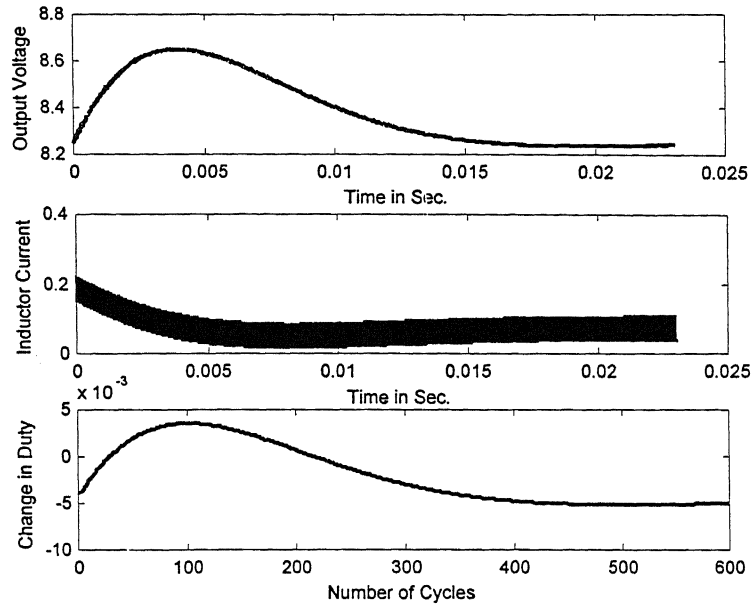


Fig. 3.27 Effect of load variation on closed loop response with Lyapunov Controller

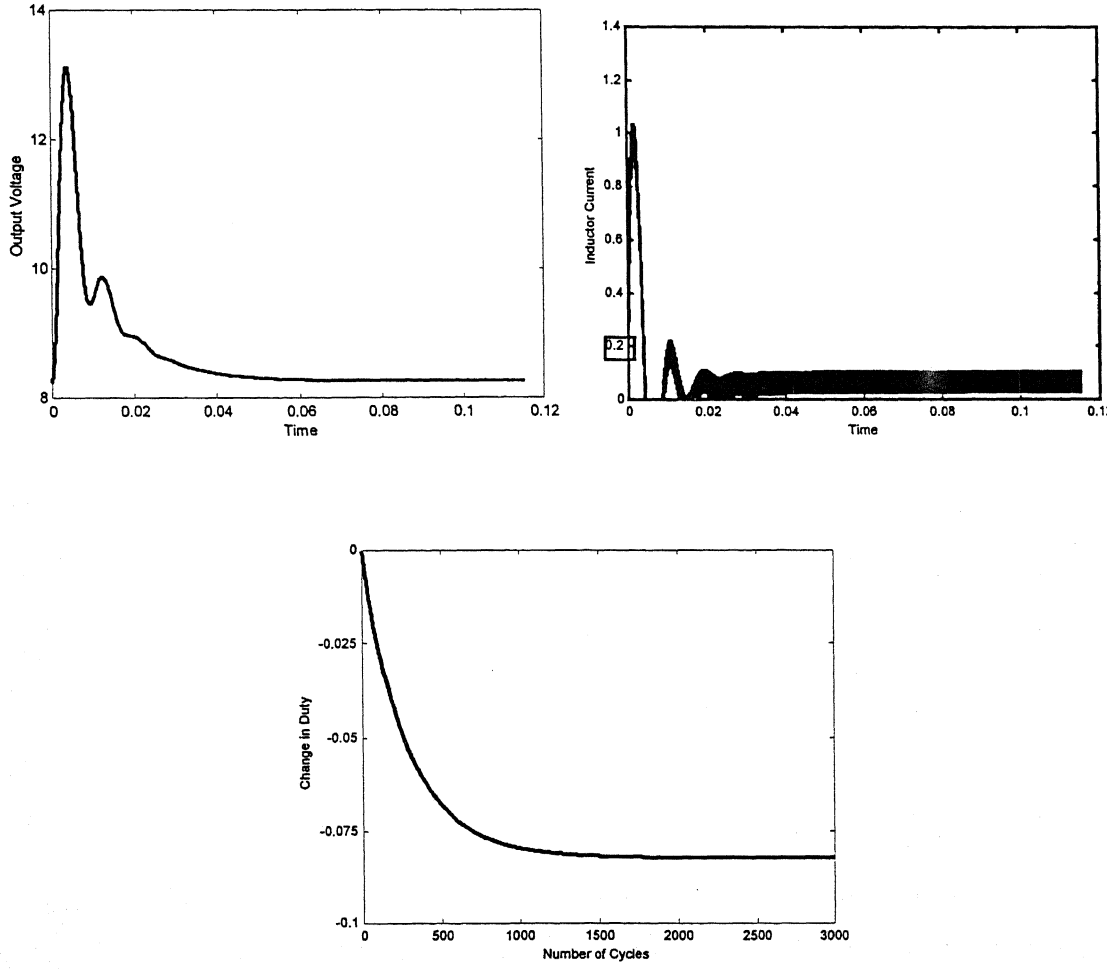


Fig. 3.28 Effect of simultaneous load and supply on closed loop response

The simulation result shown in Figs. 3.28 and 3.29 are for a simultaneous change in load and supply. The load changes from 64 Ω to 164 Ω whereas the supply changes from 20 V to 30 V at t =0. The controller although capable of these disturbances but the transient has a large overshoot and settling time becomes too high. The settling time for LQR based controller is 0.062 seconds whereas the settling time for bilinear model based controller is 0.015 seconds.

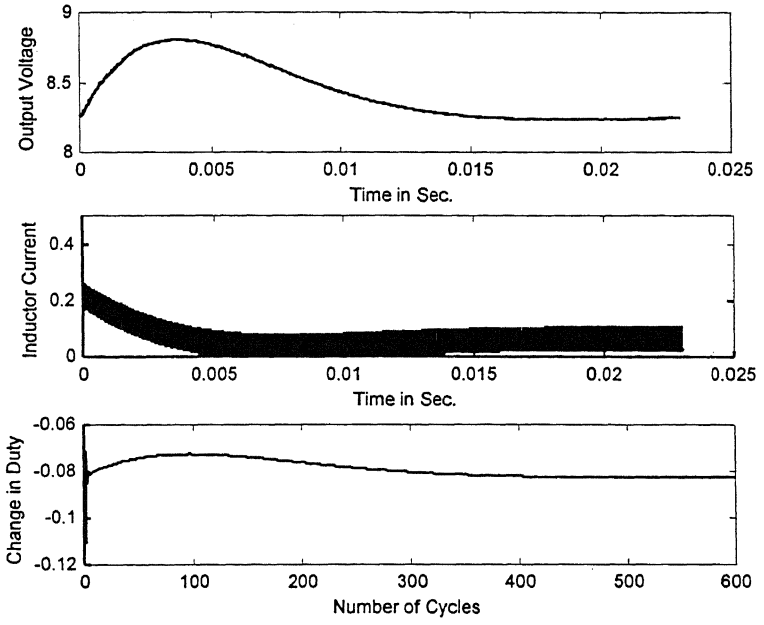


Fig. 3.29 Effect of simultaneous load and supply on closed loop response

In another simulation study, the load is changed from 64 to 10 Ohms when the converter is operating at steady state duty of 0.3. The simulated voltage, inductor current and duty ratio waveforms with both the types of the controllers are shown in Fig. 3.30 and Fig. 3.31. It can be seen from the figure that transients for LQR controller based closed loop system have comparatively larger undershoot and larger settling down as compared to bilinear model based closed loop system. The output voltage has no steady state error in both the cases.

In an another simulation study, the change in tracking command $\tilde{y}_{ref} = 15V$ and decrease in supply voltage by 10V occur at $t = 0$. The closed loop performance has been simulated with both controllers. The converter is assumed to be operating at duty ratio of 0.3 in steady state. The simulation result is shown in Fig. 3.32 and Fig. 3.33. It is evident from comparison of these figures that bilinear model based controller is better then LQR based controller.

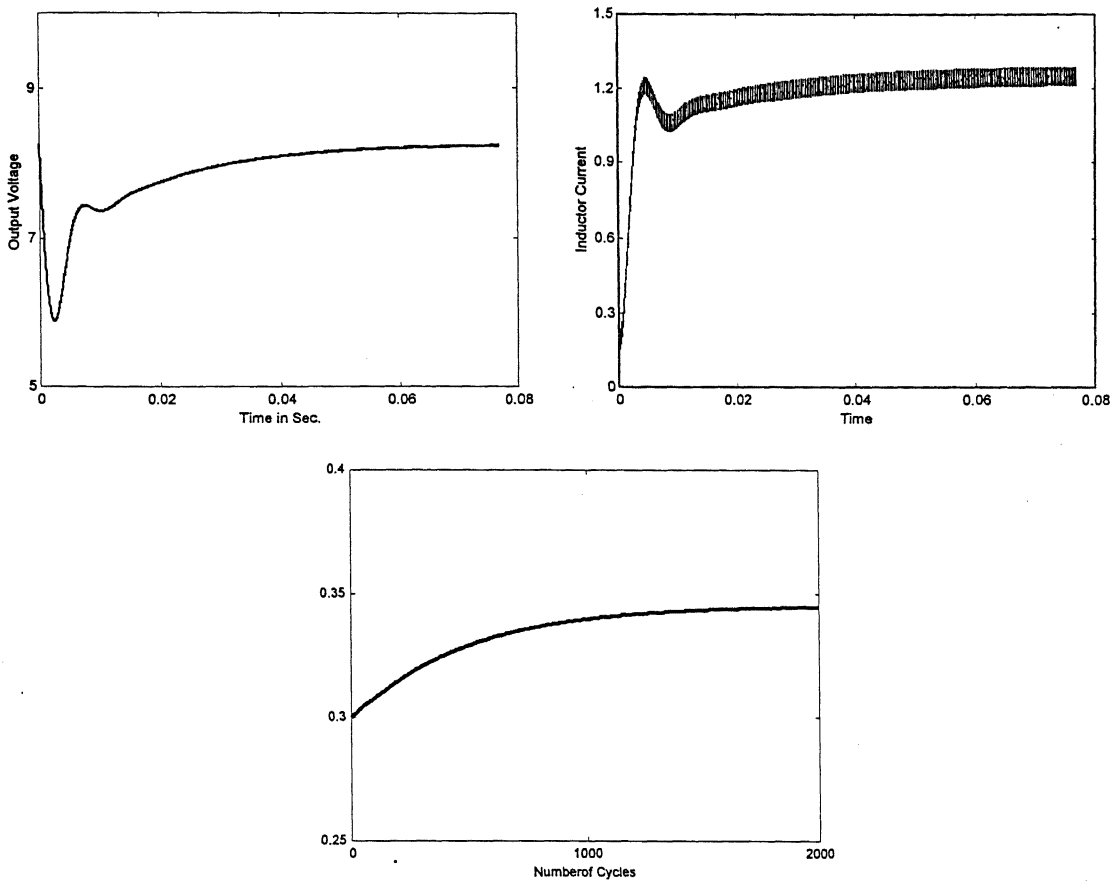


Fig. 3.30 Test results for load changed from 64Ω to 10 Ω. with LQR Controller

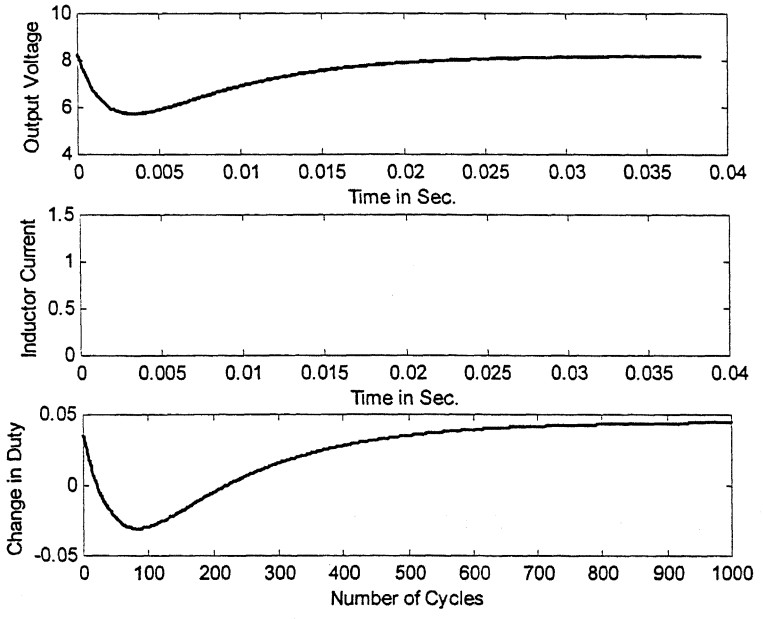


Fig. 3.31 Test results for load changed from 64Ω to 10 Ω. with Lyapunov Controller

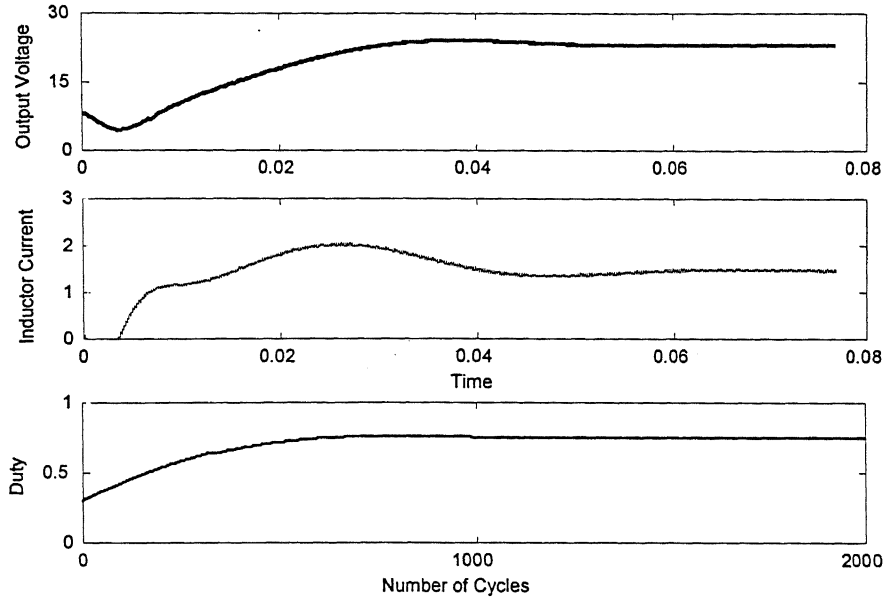


Fig. 3.32 Simulation result for tracking voltage change of 15V when the supply voltage has decreased by 10V from 20V with LQR Controller.

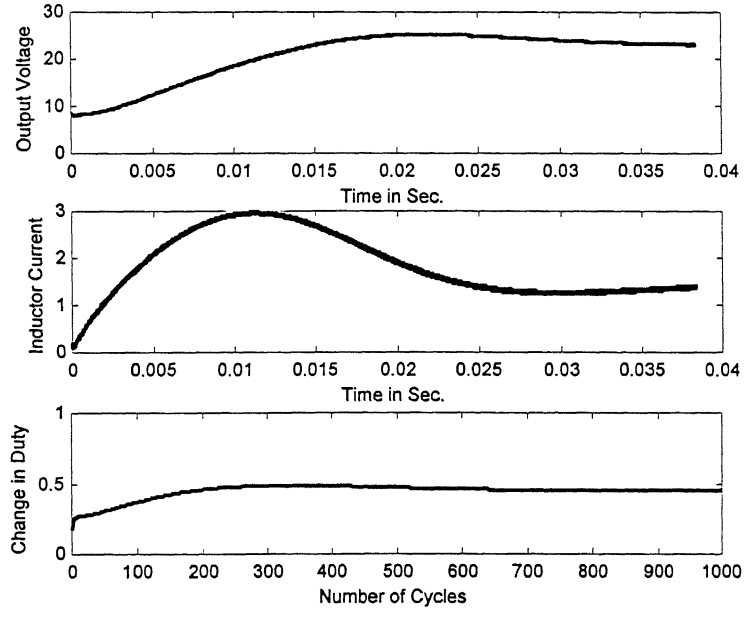


Fig. 3.33 Simulation result for tracking voltage change of 15V when the supply voltage has decreased by 10V from 20V with Lyapunov Controller.

Simulation study has been carried out for simultaneous change in load resistance, supply voltage and reference. The converter is assumed to be working in steady state with supply voltage of 20 V, load resistance of 64 Ω at duty ratio of 0.3. The steady state output voltage is 8.2 V. At $t = 0$, change in reference $\tilde{y}_{ref} = 15\,V$, load resistance decreases by 54 Ω and the input supply goes down by 10V. The simulation

results are shown in Fig.3.34 and Fig. 3.35. Both the controllers are not capable of tracking the reference and have a large steady state error.

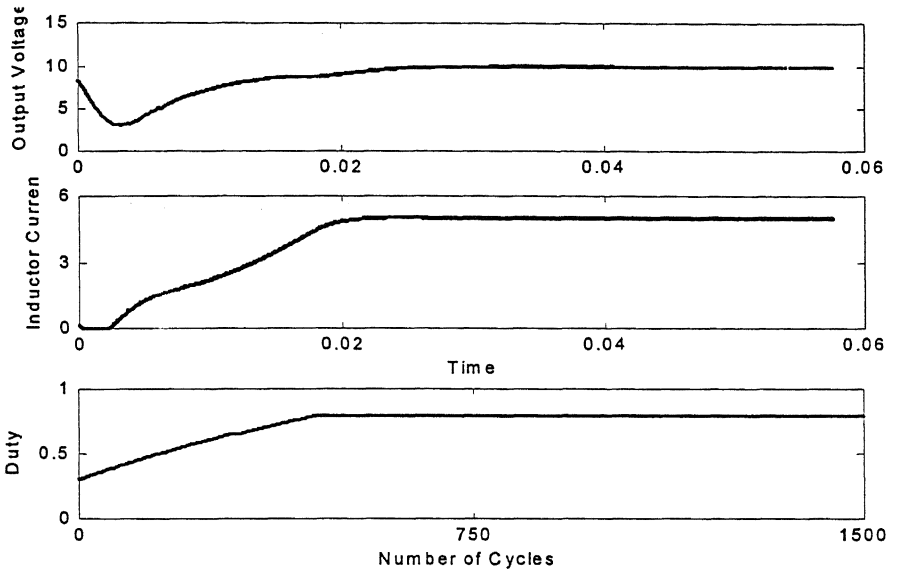


Fig. 3.34 Simulation result for tracking 15V when voltage goes down by 10V and load increases from 64 Ω to 10 Ω

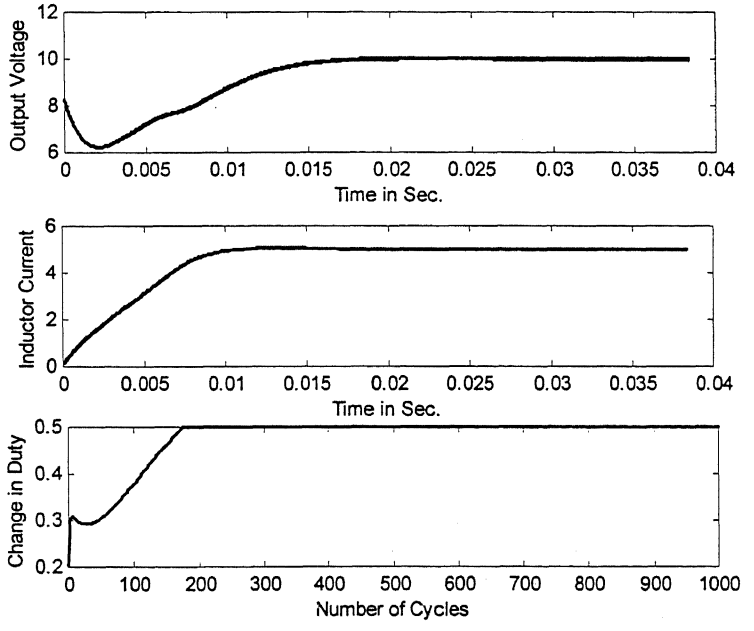


Fig. 3.35 Simulation result for tracking 15V when voltage goes down by 10V and load increases from 64 Ω to 10 Ω with Lyapunov Controller

3.4 FUZZY CONTROL

Multi-zonal modeling of nonlinear systems are generally employed to obtain a global model. One of the multi zonal models is fuzzy based Takagi-Sugeno (TS) model [64]. In this method, the nonlinear system is approximated by piece-wise linear fuzzy model in smaller zones. However, linear approximation of the system will require a large number of intervals for accurate modeling. As we have seen that the bilinear model has wider range of operation. It is therefore proposed to model the nonlinear converter by bilinear model in each of the fuzzy subintervals. The converter is described by TS model and the closed loop control law is derived by using Lyapunov stability theorem. It is expected that the closed loop system will have global stable operation.

3.4.1 Fuzzy Modeling and Control

The universe of discourse is chosen as the duty ratio space. It is divided into eight subspaces as shown in Fig. 3.36. The fuzzy IF-THEN rules are then locally represent the bilinear relations in the same manner as given by Takagi and Sugeno for linear relations [64]. For a nominal value (d_0) of duty ratio, the fuzzy system is then of the following form:

Rule-*i*: IF $d_0 \in \mathrm{A}_i$ THEN

$$\tilde{x}_i(k+1) = F_i\tilde{x}(k) + G_i\tilde{u}(k) + H_i\tilde{x}(k)\tilde{u}(k) \tag{3.17}$$

where $i = 1,\cdots,8$ and A_i is the i^{th} fuzzy set and $\tilde{u}(k)$ is the perturbation in the duty ratio acting as input to the converter. Combining all the eight zones, the final output of the fuzzy system is then given by

$$\tilde{x}(k+1) = \frac{\sum_{i=1}^{8} w_i(k)\left[F_i\tilde{x}(k) + G_i\tilde{u}(k) + H_i\tilde{x}(k)\tilde{u}(k)\right]}{\sum_{i=1}^{8} w_i(k)} \tag{3.18}$$

where w_i is the value of the i^{th} membership function. From Fig. 3.36 it is evident that a particular value of d_0 can only belong at most to two adjacent subspaces. It can be shown

that in that event $\sum w_i(k) = 1$. We can therefore rewrite (3.18) as

$$\tilde{x}(k+1) = F_W \tilde{x}(k) + G_W \tilde{u}(k) + H_W \tilde{x}(k)\tilde{u}(k) \tag{3.19}$$

where $$F_W = \sum_{i=1}^{8} w_i F_i, \quad G_W = \sum_{i=1}^{8} w_i G_i, \quad H_W = \sum_{i=1}^{8} w_i H_i \tag{3.20}$$

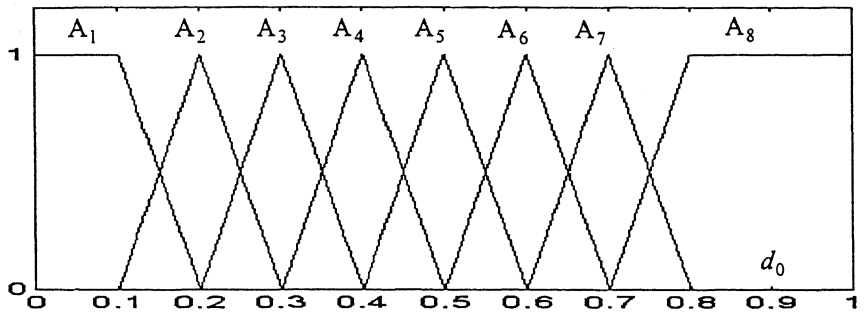


Fig. 3.36 Membership functions of TS model of the Buck-Boost converter

It is to be noted that in the above relation a maximum of two non-zero w_i's are available at any instant for a given value of d_0. The output equation in this case however is the same as that given in (3.2).

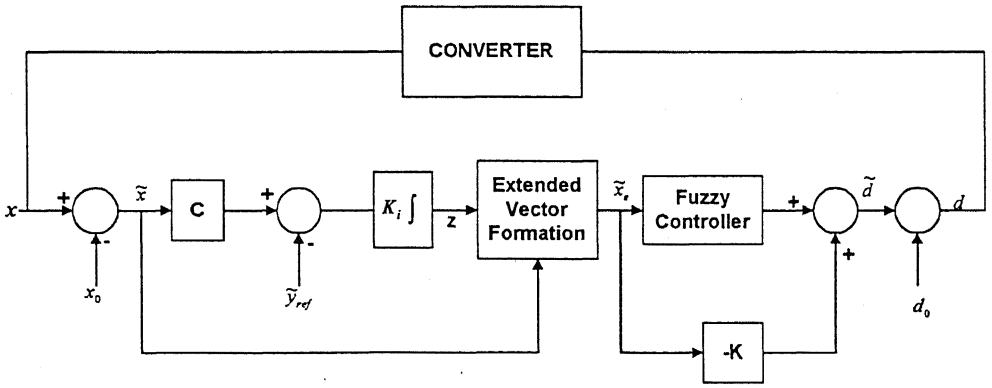


Fig. 3.37 Fuzzy Control system block diagram

In a similar way we can also weigh (2.6) and (2.8) to obtain the following matrices.

$$\Phi_{1W} = \sum_{i=1}^{8} w_i \Phi_{1i},$$

$$\Phi_{2W} = \sum_{i=1}^{8} w_i \Phi_{2i}$$

and

$$\Theta_{1W} = \sum w_i \Theta_{1i}$$

Modifying the expression for the steady state corner point as given in (2.13) we obtain a fuzzy estimate of the initial condition, given by

$$x_{0W} = [I - \Phi_{2W}\Phi_{1W}]^{-1}\Phi_{2W}\Theta_{1W}V_{dc} \tag{3.21}$$

3.4.2 Lyapunov Based Controller Fuzzy Design

The basic objective of the control design is to track a step change in the output voltage reference command or to maintain the output voltage constant for any disturbance in input voltage or load resistance. To achieve this let us introduce an auxiliary control signal of the form

$$\tilde{z}(k+1) = \tilde{z}(k) + K_i(\tilde{V}_0(k) - \tilde{y}_{ref}(k)) \tag{3.22}$$

where

$$\tilde{V}_0(k) = [1 \quad 0]\tilde{x}(k) = C\tilde{x}(k) \tag{3.23}$$

Let us define an extended state vector as $\tilde{x}_e^T = [\tilde{x}^T \quad \tilde{z}]$ and combine (3.23), (3.22) and (3.19) to get

$$\tilde{x}_e(k+1) = F_1\tilde{x}_e(k) + G_1\tilde{u}(k) + H_1\tilde{x}_e(k)\tilde{u}(k) + J_1\tilde{y}_{ref}(k) \tag{3.24}$$

where

$$F_1 = \begin{bmatrix} F_W & \begin{bmatrix}0\\0\end{bmatrix} \\ K_iC & 1 \end{bmatrix}, G_1 = \begin{bmatrix} G_W \\ 0 \end{bmatrix}, H_1 = \begin{bmatrix} H_W & \begin{bmatrix}0\\0\end{bmatrix} \\ [0 \quad 0] & 0 \end{bmatrix}, J_1 = \begin{bmatrix} 0 \\ 0 \\ -K_i \end{bmatrix}$$

The closed loop controller has been designed as done in Subsection 3.2.2. The control law has two parts. One is a pole placement controller, while the other is augmented input derived by applying Lyapunov stability theorem. The control law (3.17) is reproduced below.

$$\tilde{u}(k) = -L\tilde{x}_e(k) + v(k)$$

Substituting (3.25) in (3.24) we get

$$\begin{aligned}\tilde{x}_e(k+1) = F_e\tilde{x}_e(k) + G_e v(k) + H_e\tilde{x}_e(k)v(k) \\ + J_e\tilde{y}_{ref}(k) - H_e\tilde{x}_e(k)L\tilde{x}_e(k)\end{aligned} \tag{3.26}$$

where $F_e = (F_1 - G_1 L);\ G_e = G_1,\ H_e = H_1,\ J_e = J_1$.

Let us consider a Lyapunov function of the form $V(k) = \tilde{x}_e^T(k)P\tilde{x}_e(k)$. Substituting $\tilde{x}_e(k)$ from (3.26), we get the difference function of

$$\begin{aligned}\Delta V(k) &= V(k+1) - V(k) \\ &= \tilde{x}_e^T(k)\left[F_e^T P F_e - P\right]\tilde{x}_e(k) + \Im\left(\tilde{x}_e(k), v(k)\right)\end{aligned}$$

where $\Im\left(\tilde{x}_e(k), v(k)\right)$ is the collection of all remaining terms. We now choose the P matrix above such that $F_e^T P F_e - P$ is negative definite and minimize the function $f\left(\tilde{x}_e(k), v(k)\right)$ to obtain the $v(k)$ given by (3.27).

$$v(k) = -\frac{\tilde{x}_e^T(k)F_e^T P\left[G_e + H_e\tilde{x}_e(k)\right] + \left[G_e^T + H_e^T\tilde{x}_e^T(k)\right]\eta(k)}{G_e^T P G_e + \tilde{x}_e^T(k)H_e^T P\left[H_e\tilde{x}_e(k) + 2G_e\right]} \tag{3.27}$$

where $\eta(k) = J_e\tilde{y}_{ref}(k) - H_e\tilde{x}_e(k)L\,\tilde{x}_e(k)$.

This derivation is similar to the one given in Appendix B.2.

Lemma: Let the dynamic equation of the system is given by (3.18) for a multi zonal fuzzy system, where w_i are the membership functions of state variables in respective zones. If there exists a positive definite common matrix P such that

$$F_i^T P F_i - P < 0, \quad i = 1,\ldots,n \tag{3.28}$$

The dynamic system given by (3.18) is closed loop stable. The proof of the lemma is given in [65].

The simulation study has been carried out with control law for the closed loop operation of the Buck-Boost converter. A common P is obtained by trial and error method satisfying (3.28) for all the eight F_i. This P is used in (3.27) to calculate the control action. The control action does not require any defuzzification. The simulation results are given below in Fig. 3.38 to Fig. 3.40.

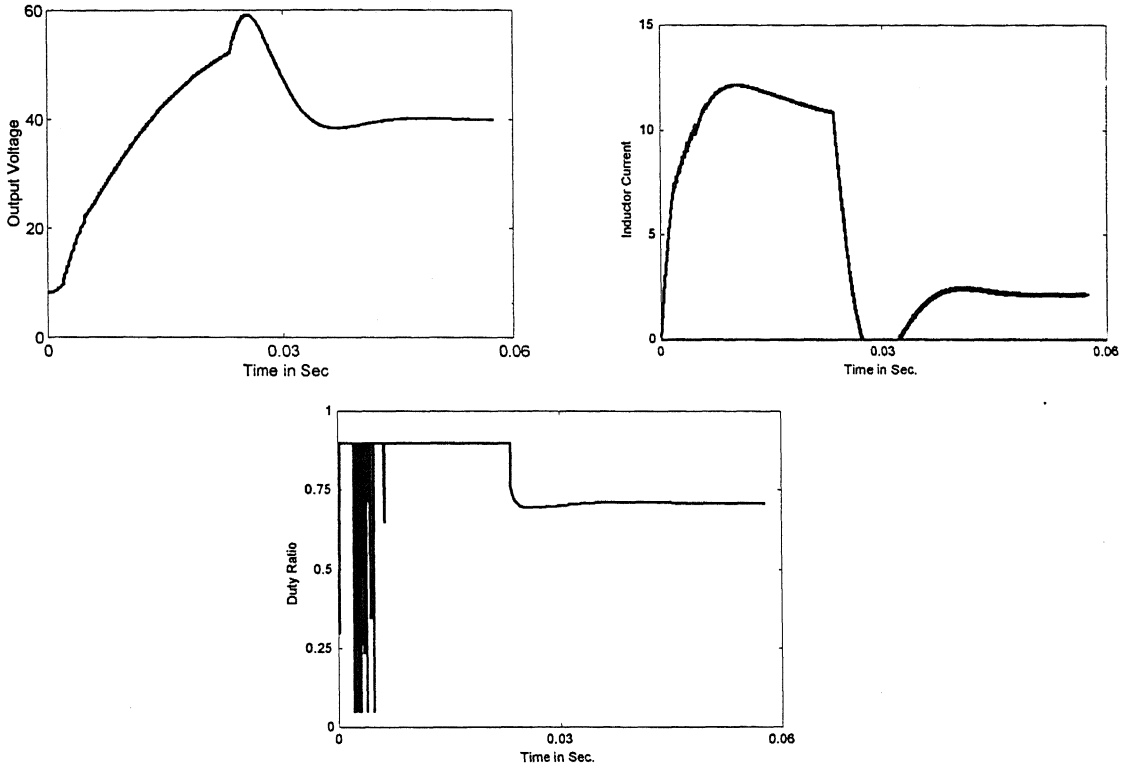


Fig. 3.38 Simulation result for tracking of 32 V with Fuzzy Controller.

The supply voltage and load resistance is respectively 20V and 64 Ω. The converter is operating at 26 kHz. The converter is operating at a duty ratio of 0.3 in steady state. The reference command $y_{ref} = 32V$ is issued at $t = 0$. The simulation results are shown in Fig. 3.38. The duty ratio saturates at 0.9 and the capacitor voltage and inductor current builds up. The duty ratio has bang-bang characteristics in the transient followed by again saturation of the duty ratio. It is to be noted that the converter during transient traverses through different fuzzy zones before settling down finally in any one of the fuzzy zone. The converter settles down to steady state duty ratio of 0.6875 and the output voltage goes to 40V, the desired output voltage. The peak overshoot is of the order of supply voltage 20V. The fuzzy

controller has a poorer dynamic response compared to the controller based on bilinear model shown in Fig. 3.16.

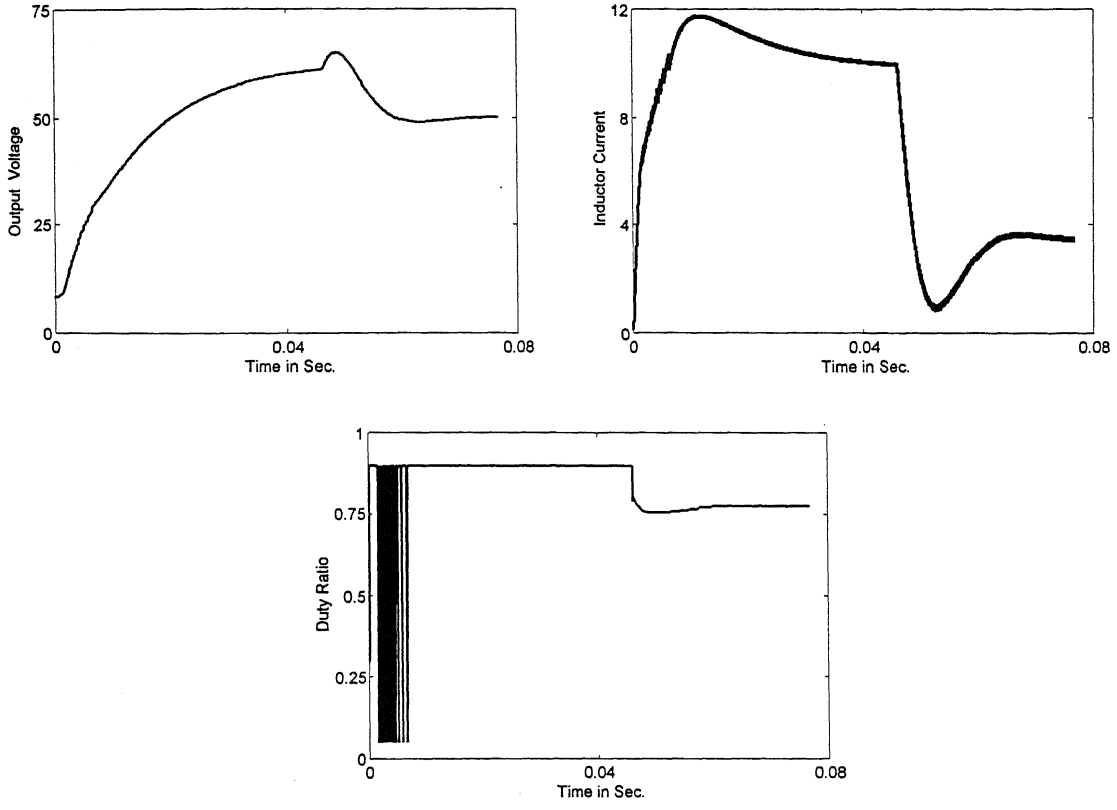


Fig. 3.39 Simulation result for tracking of 42 V.

The fuzzy controlled system has been tested for tracking command of 42 V. The simulation results are shown in Fig. 3.39. The converter has a poor dynamic response, but it is capable of tracking the voltage. The converter is capable of tracking larger voltage changes than 42 V. The fuzzy controller fails to track 75 V change in the reference command. The result is shown in Fig. 3.40. The duty ratio saturates and stays permanently at this value. However, the tracking performance has been tested up to 60 V (300 % of supply voltage) and the closed loop converter system is capable of tracking these changes. The results of these simulations are not given here.

The closed loop performance for load and supply disturbances have similar type of jitter in duty ratio and the dynamics is sluggish. Thus, these results are not presented here.

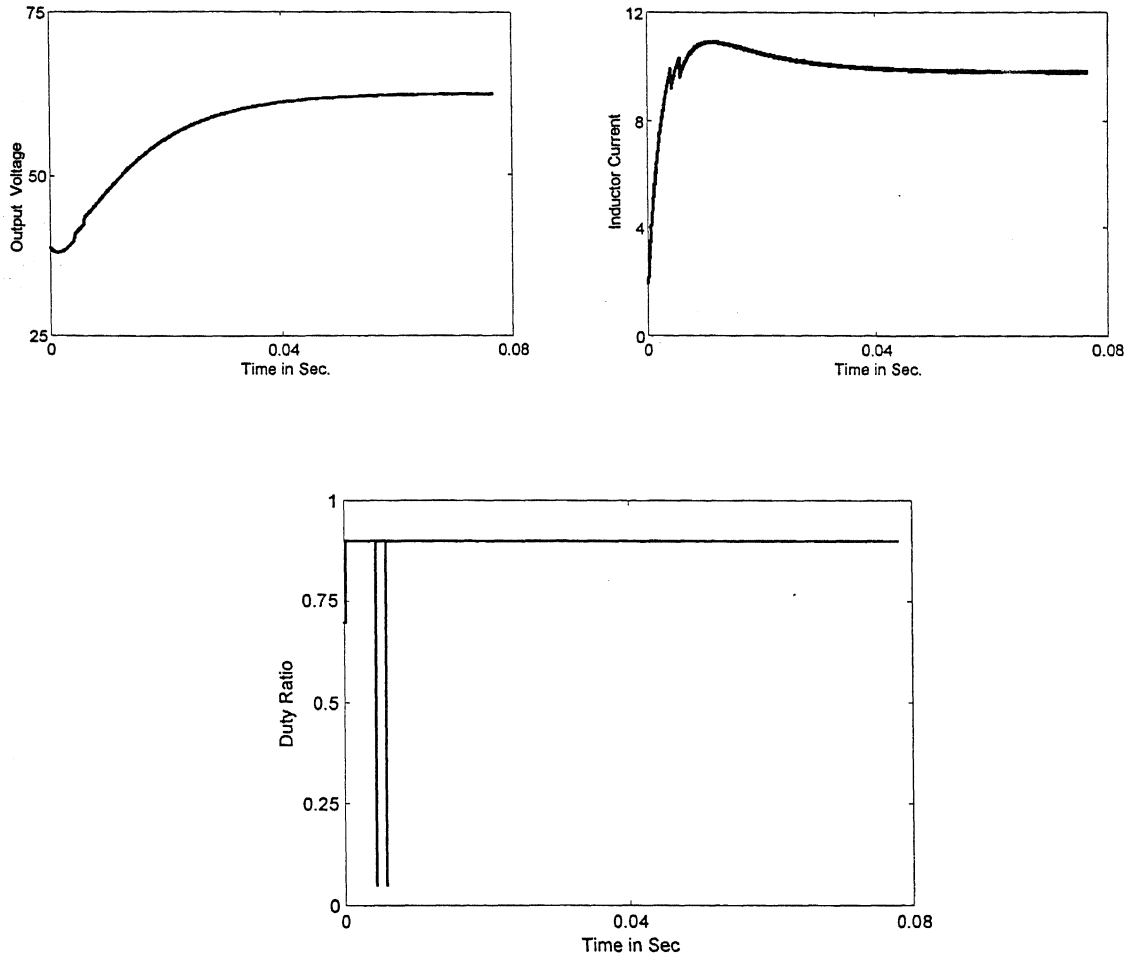


Fig. 3.40 Simulation result for tracking of 75 V. Output remains at 62V.

3.5 CONCLUSION

Experimental and simulation study has been carried out to verify the closed loop operation of Buck-Boost converter. Five different controllers that work in linear, bilinear and fuzzy domain are designed. These controllers are fairly robust and can track large changes in the output voltage. Fuzzy controller has better tracking performance compared to others. Out of all controllers, the controllers designed using the Lyapunov's stability theorem using the bilinear model have the smoothest control action.

In Chapter 2 we have discussed various models and proposed a new bilinear model that has a better accuracy. In this chapter we have designed controllers based on the bilinear as well as linear models. However it can be seen that the maximum change in the

output that can be tracked by these controllers is limited to 175 %. Also for tracking large voltage change , the system response becomes sluggish. Therefore we can conclude that the system performance cannot be improved further with the present topology. Some minor improvement can be achieved by using more complicated controllers. Thus for better system performance, we need to modify the topology of the converter. This is discussed in next chapter.

CHAPTER 4

MODIFIED TOPOLOGIES:

STEADY STATE OPERATION AND SMALL SIGNAL MODELING

A conventional Buck-Boost converter shown in Fig. 2.2 has one controlled switch in the input side which allows the inductor current to rise or fall to the desired levels. But, the diode in the output circuit forces the output capacitor to be charged for the entire OFF period of the controlled switch. The regulation of the capacitor voltage is possible only by changing the OFF period of the switch, which is complement of the ON period if the converter is operating in CCM. Therefore the control of the output voltage is not direct.

There are primarily three types of disturbances possible in any converter. These are input or source deviation from its nominal value, load vacillation from its rated value and parameter alteration. These disturbances may be due to various possible reasons, such as poor source regulation, rapidly changing loads, saturation of magnetic core, etc. The input supply variations can be retracted optimally in time [54], often in one cycle by controlling the switch of the conventional converter. To take into account parameter variation

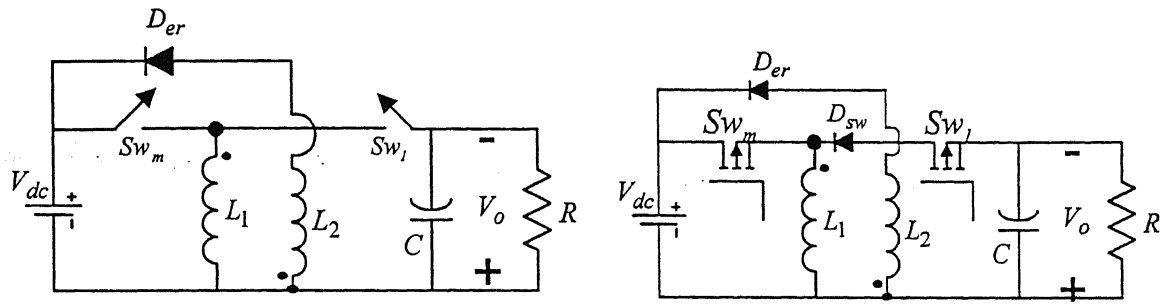
alongwith other control objectives, adaptive or robust controller has been extensively used in literature [47,50]. However, the topology of such systems is designed for desired steady state performance and therefore the system dynamic response is normally poor. Even if the time optimization of the response is done, the natural circuit time constant cannot be reduced and hence faster operation beyond a limit is not feasible. The natural time constant of the circuit is a function of inductance, capacitance and load resistance of the converter. It is to be noted that these circuit parameters are not designed for performance indices of closed loop controller. The parameter values are chosen such that the steady state performance criteria of the converter are met. Thus, the dynamic response of conventional Buck-Boost converter does not improve beyond a limit due to topological limitations. A topology is therefore required for rejection of the various disturbances in optimal time.

4.1 MODIFIED CONVERTER TOPOLOGY

Keeping above in view, we propose a two-switch flyback dc-dc converter, which is shown in Fig. 4.1 (a). In this converter topology, the switch Sw_1 has replaced the diode of the conventional Buck-Boost converter on the load side. This switch allows controlled charging of output capacitor connected across the load. The controlled charging may require simultaneous opening of both the switches. To facilitate simultaneous opening of both the switches, an energy recovery winding with a third switch Sw_2 (not shown) or a diode called energy recovery diode D_{er} has been provided. However, an alternate solution for disconnecting the output capacitor from inductor is to connect a second switch Sw_1 across the inductor [55] during OFF interval of Sw_m. The switch in this configuration carries the inductor current corresponding to full load and therefore may have large ON state losses in addition to the switching losses. Whereas the circuit proposed requires special design for coupled inductor.

A non-ideal coupled inductor may have appreciable amount of leakage inductance, which causes oscillation with stray capacitance of the windings. Special measure has to be taken to counter these parasitic oscillations. The necessary measures or modification or alteration in basic topology shown in Fig. 4.1 may compensate parasitic oscillation. Besides

these, other issues like evaluation of loss and determination of the converter parameters has been left for future work.



(a) (b)

Fig. 4.1 Proposed two-switch flyback converter

The switch Sw_1 is realized in hardware by series combination of power MOSFET Sw_1 and high-speed diode D_{sw} as shown in Fig. 4.1 (b). The series diode D_{sw} although looks redundant is essential. The simulation study of converter with only power MOSFET in place of switch Sw_1 has been carried out in PSPICE. It has been observed that the MOSFET switch Sw_1 conducts with main switch Sw_m even when the gate signal for Sw_1 is not applied. This inspired use of diode in series with MOSFET. The hardwired experiment also conforms to simulation result. Thus the realization of load switch Sw_1 has been done by series combination of MOSFET and diode. All the power MOSFETs and power diodes used in converter circuit has snubber circuits in parallel to the devices. It is interesting to note that the use of snubber circuits across devices reduces the parasitic oscillation [3].

Let the number of turns in the winding of inductance L_1 be N_1 and that of L_2 is N_2. Let us also define $a = N_1 / N_2$ as the turn ratio of the coupled inductors L_1 and L_2. By transformer action, the voltage across energy recovery winding will be aV_0. The forward voltage difference across energy recovery switch Sw_2 is $V_{Sw_2} = aV_0 - V_{dc}$. The forward voltage V_{Sw_2} is negative if $V_0/V_{dc} > a.$ and therefore a fast recovery diode D_{er} can be used to realize the switch Sw_2 in Fig. 4.1 (b). Otherwise a series combination of diode and power MOSFET as has to be employed to realize Sw_2 as done for Sw_1. We shall call D_{er}

as the energy recovery diode.

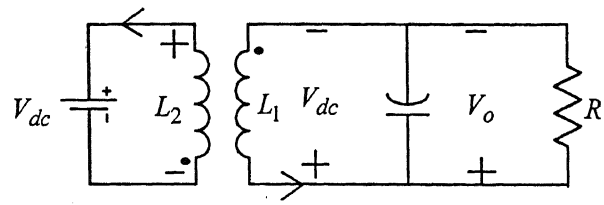


Figure 4.2: Simultaneous conduction of load switch and energy recovery diode

If diode D_{er} is retained when $V_0/V_{dc} > a.$, it will result into simultaneous conduction of load switch and energy recovery winding as shown in Fig. 4.2. This will force two different voltages to the transformer windings. The energy recovery winding will be at a voltage V_{dc} and main winding will be at output voltage V_o. As a result of simultaneous conduction of load switch and the energy recovery diode, the capacitor will be forced to charge to input voltage and diode will experience short circuit. This is true for converter operating in either buck or boost mode. It is therefore necessary to have third controlled switch in place of diode for this condition. The third switch has been assumed where ever required in all the simulation studies carried out in this chapter.

The converter is assumed to operate in continuous conduction mode (CCM) at constant frequency. Further, it is assumed that the converter operates with low ripple in voltage and core mmf. The average output voltage and core mmf over a cycle may be assumed to be a pure DC quantity. Under these conditions, the steady state analysis of the proposed converter can be carried out by averaging technique [6].

4.2 OPERATION OF CONVERTER

The direction of the instantaneous currents i_{L1} and i_{er} are shown in Fig. 4.1 (b). The core mmf is defined as $\Im = N_1 i_{L1} + N_2 i_{er}$. Fig. 4.3 shows the waveform of the converter operating at constant frequency $(1/T)$ in CCM. The main switch Sw_m is closed at the beginning of each cycle, for a time DT. Note that D in this chapter refers to duty ratio of the main switch Sw_m. In the previous chapters D had been used to represent diode. The

diodes in this chapter are represented by D with appropriate suffix, e.g. D_{er} for energy recovery diode. During this time current i_{L1} and hence the mmf $\Im$ increase linearly, while the capacitor C discharges through load resistance. At time DT switch Sw_m is opened and Sw_l is closed. The switch Sw_l remains on for duration of $d\,T$. During this interval the stored magnetic energy of inductor is transferred to the capacitor and the output voltage (v_0) increases. At time $(D+d)T$ the switch Sw_l is opened. As both the switches are open, the current in L_1 is transferred to L_2 to maintain continuity of the core mmf and the energy recovery interval begins. The energy recovery continues till the end of the cycle. The capacitor supplies the load current during this time interval. Figs. 4.4 (a) to 4.4 (c) show the equivalent circuits for operation with various switch closures. Fig. 4.4 (a) is the equivalent circuit of the converter circuit when main switch Sw_m is closed, Fig. 4.4 (b) is similarly the equivalent circuit when Sw_l conducting and 4.4 (c) is for energy recovery interval.

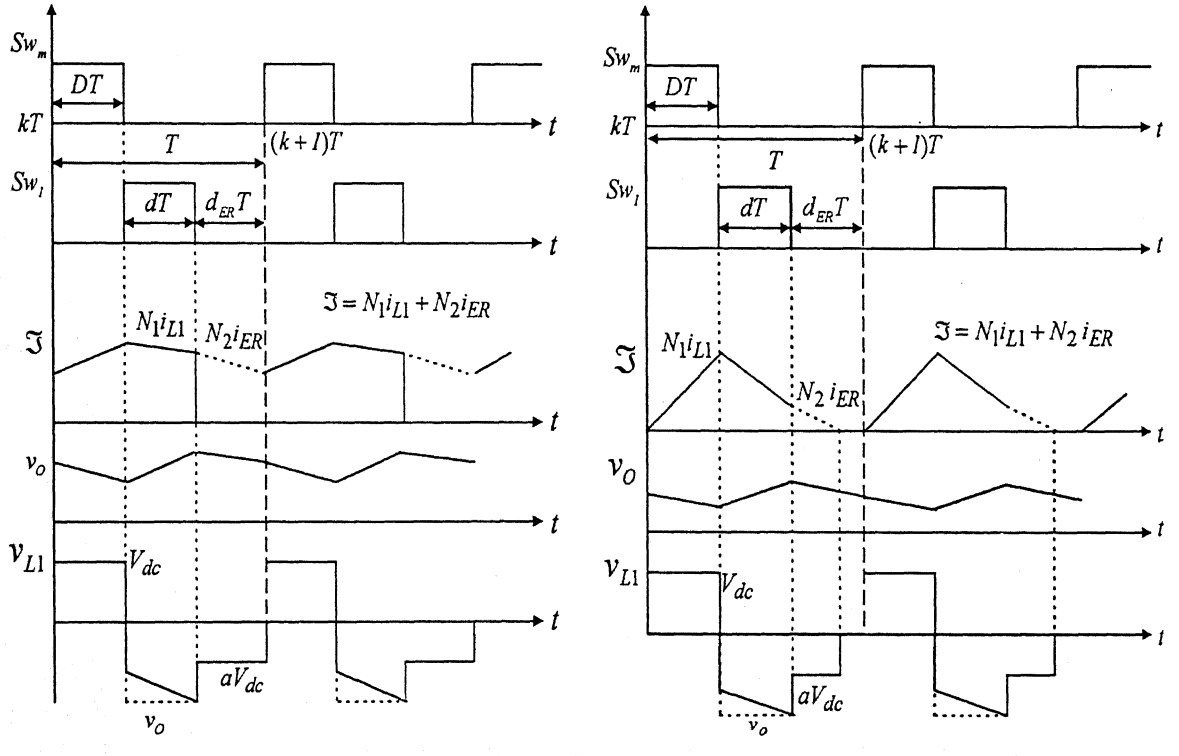


Fig. 4.3 Switching diagram of the modified Buck-Boost converter in (a) CCM (b) DCM

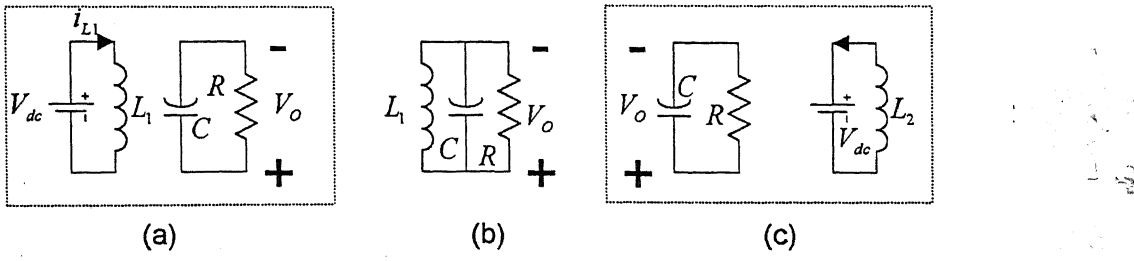


Fig.4.4 Equivalent circuits of the flyback converter: (a) Sw_m conducting, (b) Sw_1 Conducting, and (c) energy recovery in CCM mode

In discontinuous conduction mode (DCM) of operation, the circuit behavior is similar to that described above in the continuous conduction mode, except that the current in the inductor L_2 and therefor the core mmf drops to zero during energy recovery operation. The initial value of i_{L1} is thus always zero at the beginning of each cycle. The relevant voltage and current of the converter operating in DCM is shown in Fig 4.3 (b). Although, the core mmf has a large ripple, the output voltage may have smaller ripple content at higher frequencies for suitably chosen converter parameters. The average value of the converter states may be assumed constant over a switching cycle. Therefore averaging method may also be applied for the analysis of the converter in DCM mode. The equivalent circuits for different ratios are shown in Figs. 4.5 (a) to 4.5 (d). Figs. 4.5 (a) to Fig. 4.5 (c) is analogous to the CCM mode intervals and Fig. 4.5 (d) represents DCM interval. It is to be noted that the segment of waveform for the voltage across the inductor v_{L1} represented by dotted line in Figs. 4.3 (a) and 4.3 (b) are based on the small ripple approximation, whereas the actual voltage across the inductor v_{L1} is shown by solid lines.

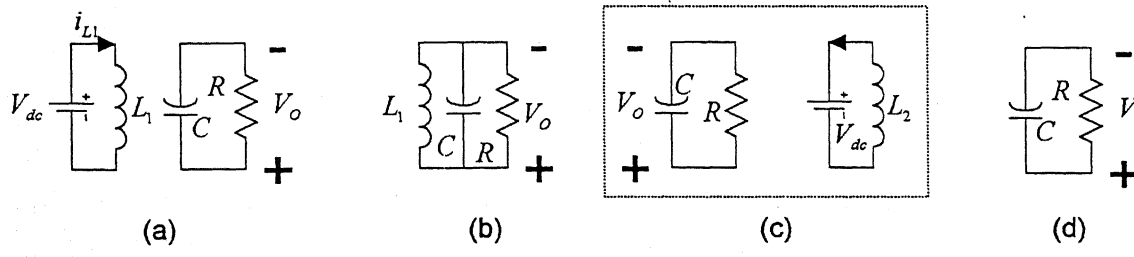


Fig. 4.5 Equivalent circuits of the flyback converter in DCM: (a) Sw_1 conducting, (b) Sw_2 Conducting, and (c) energy recovery (d) all switch OFF

4.3 STEADY STATE CHARACTERISTICS OF CONVERTER FOR CONSTANT FREQUENCY OPERATION

By the steady state characteristics of the converter, we mean relationship between voltage gain, defined as the ratio of output voltage and input voltage, and duty ratio of the converter. These characteristics have been derived here using averaging technique. The converter is assumed to operate at a high frequency and hence they have small ripple in output voltage and core mmf. The averaging technique assumes the average over a cycle is equal to average over subintervals. The averaging technique normally employs two fundamental principals, namely

1. Voltage-Second balance across inductor
2. Charge balance for capacitor

For a converter operating in steady state the voltage-second product across the inductor, which is equal to net change in core flux over a cycle, must be zero. Similarly, net increment in capacitor charge must be zero over a cycle in steady state.

The increment in flux takes place when the inductor is connected to dc source and it reduces when the stored magnetic energy of the inductor is used for charging capacitor connected across the load and during the energy recovery interval. The voltage waveform across the inductor represented by v_{L1} is shown in Fig. 4.3 (a). The magnitudes of the average inductor voltage in different duty intervals are marked in the figure. Applying volt-sec balance across the inductor gives

$$V_o dT + aV_{dc} d_{ER} T = V_{dc} DT \tag{4.1}$$

Where $a = N_1 / N_2$ is the turn ratio of the coupled inductors as stated above. Inductors L_1 and L_2 are assumed to be tightly coupled and there is no leakage. The quantity d_{ER} appearing in (4.1) is the energy recovery duty ratio and for the CCM operation, it must be equal to $1 - D - d$. Solving (4.1) and using $d_{ER} = 1 - D - d$, we obtain the output voltage as

$$\frac{V_0}{V_{dc}} = a + \frac{(a+1)D - a}{d} \tag{4.2}$$

In steady state, net charge accumulation for the capacitor in the interval dT_s must be equal to charge supplied by the capacitor to load in the interval $(1-d)T_s$. We call this principle of charge balance for the capacitor. Let the instantaneous output voltage and core mmf are represented by v_0 and $\Im$. The average core mmf over a cycle will be then be given by

$$F_{av} = \frac{1}{T}\int_0^T \Im(t)dt$$

If I_{L1} is the average of instantaneous inductor current i_{L1} and I_{er} is average of instantaneous energy recovery current i_{er}, then it can be shown that $F_{av} = N_1 I_{L1} + N_2 I_{er}$. The instantaneous output voltage (v_0) and core mmf $\Im$ are assumed to be equal to the average output voltage (V_o) and core mmf $\Im_{av}$ respectively due to small ripple over a cycle. Therefore, the charge balance on the capacitor can be written as

$$\left[\frac{F_{av}}{N_1} - \frac{V_o}{R}\right]dT = \frac{V_o}{R}(1-d)T \tag{4.3}$$

Solving (4.3) we get

$$F_{av} = N_1\left(\frac{1}{d}\right)\left(\frac{V_0}{R}\right) \tag{4.3a}$$

Equation (4.3a) can be used for determining the average mmf of the core in terms of rated voltage, loading, number of main inductor turns and load duty ratio. This helps in obtaining the core dimension and length of the air gap required to avoid magnetic saturation.

The modified Buck-Boost converter can be operated in all possible modes such as buck, boost or Buck-Boost mode. For buck operation of the converter, $V_0/V_{dc} \le 1$. Solving (4.2), we get the following conditions for buck mode of the operation of the converter.

$$a+\frac{(a+1)D-a}{d}\leq 1$$

If the converter is operated at a constant D or a constant d, the buck mode of the converter requires the following conditions to be fulfilled.

At given value of D $$d\leq \frac{a}{a-1}-\frac{(a+1)}{a-1}D \tag{4.4}$$

Similarly, at given value *d*, $$D\leq \frac{a}{a-1}-\frac{(a-1)}{a+1}d \tag{4.5}$$

It is to be noted that (4.4) is only necessary condition but not the sufficient condition as the quantity on the right of the inequality must be positive number and should be less than $(1-D)$. Applying this condition, we get

$$0\leq \frac{a}{a-1}-\frac{(a+1)}{a-1}D<1-D \tag{4.6}$$

Thus, for buck mode operation of the converter at a given main duty D, (4.4) and (4.6) must be satisfied simultaneously. Equation (4.6) also gives us limits on main duty by simplification.

$$\left.\begin{aligned} D_{\min} &= 0.5 \\ D_{\max} &= \frac{a}{a+1} \end{aligned}\right\} \tag{4.7}$$

In the similar way, solving (4.5), we get (4.8) and (4.9), which are the limiting conditions of load duty for buck mode operation for a given load duty *d*.

$$0\leq \frac{a}{a-1}-\frac{(a-1)}{a+1}d<1-d \tag{4.8}$$

$$\left.\begin{aligned} d_{\min} &= \frac{a(a+1)}{(a-1)^2} \\ d_{\max} &= \frac{(a^2-1)}{2} \end{aligned}\right\} \tag{4.9}$$

Similar limits can be obtained for boost operation of the converter.

To study the dependence of the converter voltage gain on the duty ratios for a given turns ratio we need a three-dimensional (3-D) plot. This is shown in Fig. 4.6 for a turns ratio (a) of 3/2. The hilly surface in the figure represents the feasible voltage gain for converter operating in CCM. The flat 2-D surface is either representing DCM operation of the converter or infeasible operation (regions are marked in Fig 4.6). It can be easily seen from the figure that the converter with a turn ratio of 1.5 can be operated in buck and boost mode in CCM. The maximum voltage gain for this case is approximately 7.

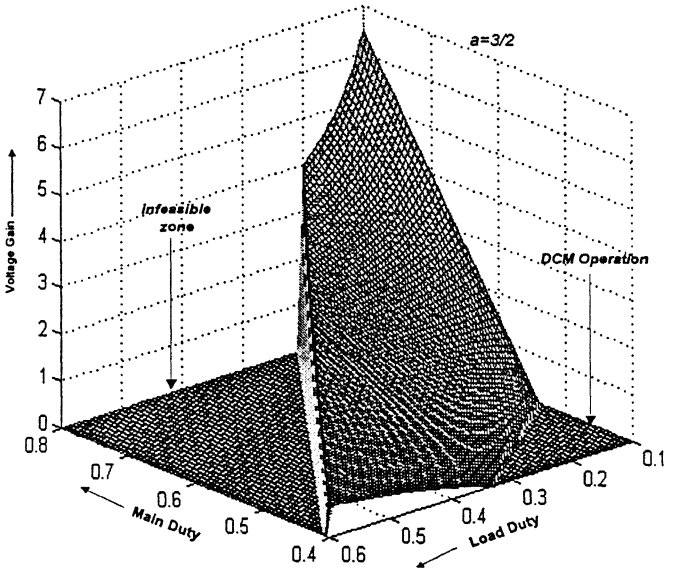


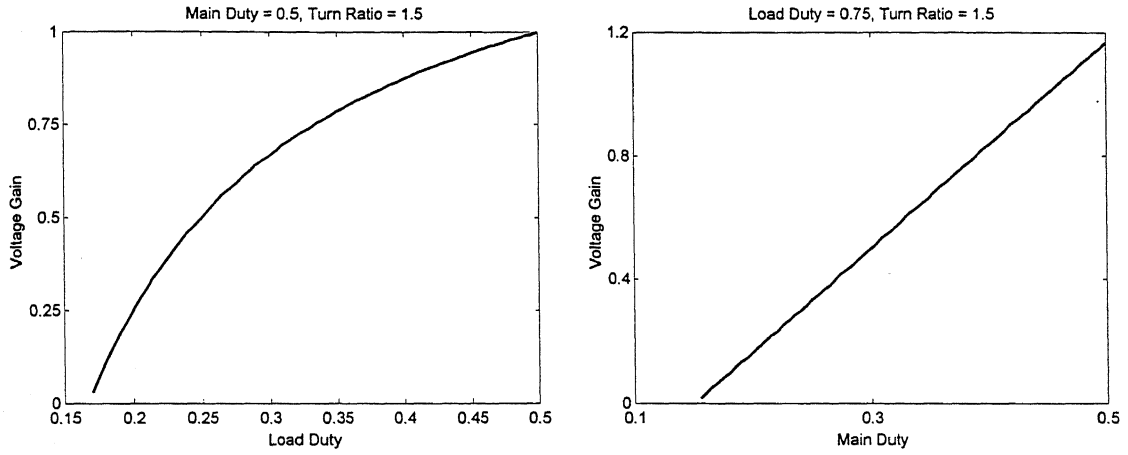
Figure 4.6. Steady state characteristics of modified converter for a=1.5

Fig. 4.7 is one of the numbers of possible section diagram of 3-D plot shown in Fig. 4.6. Fig. 4.7 (a) is section taken at constant main duty D = 0.5, while Fig. 4.7 (b) is drawn for a constant load duty d of 0.75. It can be seen from Fig. 4.7 (a) that the voltage gain of the converter increases with increase in load duty at constant main duty. Whereas Fig. 4.7 (b) clearly shows that increasing main duty at constant load duty also increases the output voltage gain. The relationship with main duty is however seems to be more linear compared to load duty variation.

The converter characteristic for a different turns ratio (a = 2.5) is shown through the

3-D plot of Fig. 4.8. Comparing this figure with Fig. 4.6, we can conclude

- The 3-D surface for these two turns ratios are almost identical. This implies that the nature of voltage gain of the output remain almost the same for different turn ratios with main duty control and load duty control.
- With the increase in the turn ratio, the maximum gain reduces. Thus, a high gain converter operating in CCM must be designed with smaller turn ratio.
- The zone of CCM operation gets narrower with the increase in turn ratio.



(a) (b)

Fig. 4.7 Effect of (a) Load duty and (b) Main duty on voltage gain at constant Main duty and Load duty respectively.

Fig. 4.9 depicts the section of the 3-D plot of Fig. 4.8 that is for a main duty (D) of 0.5. A comparison of this figure with Fig. 4.7 (a) reveals that the rate of rise of voltage gain with load duty is less for converter with larger turn ratio. Nevertheless, the nature of rise of voltage has almost the same shape for both the cases.

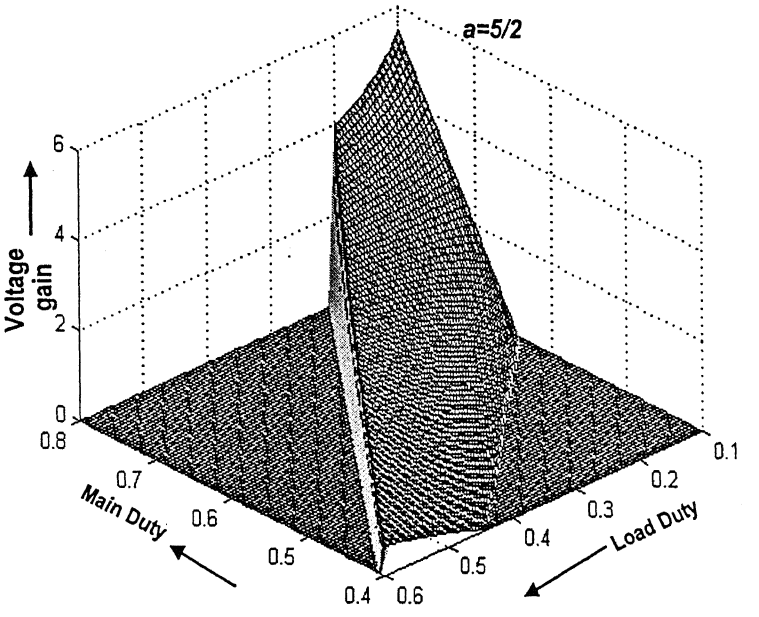


Figure 4.8. Steady state characteristics of modified converter for a=2.5

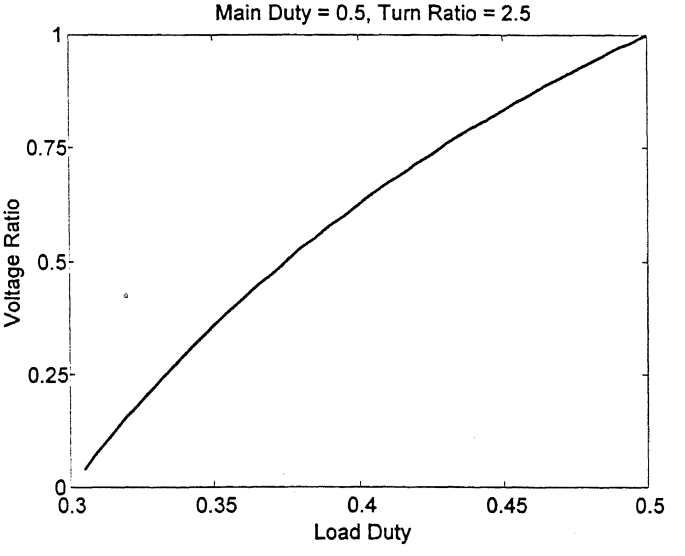


Fig. 4.9 Steady state characteristics of modified converter. Effect of load duty on voltage gain at a constant main duty.

4.4 SIMULATION AND EXPERIMENTAL VERIFICATION

Hardwired experiments have been carried out in the laboratory to verify the steady state characteristics discussed earlier. For this, a low power converter has been made in the laboratory. The detail of the realization of the converter and its controllers are given in Chapter 6. The parameters of the converter are as follows.

$$L_1 = 3.54 \text{ mH}, \quad C = 330\ \mu\text{F}, \quad R = 18\ \Omega, \quad V_{dc} = 20 \text{ V}, \quad a = 3/2$$

The dynamics of the converter have been simulated by state space method using the above parameters. Let us denote the instantaneous mmf of the core containing both the main and energy recovery windings as F and output voltage v_o. Defining a state vector x as

$$x^{\mathrm{T}} = [v_0 \quad \Im]$$

From Fig. 4.4, the state space dynamic equation for three duty intervals are written as

$$\dot{x} = A_1 x + B_1 V_{dc} \quad \text{for} \quad Sw_m \text{ ON}, Sw_1 \text{ OFF and } D_{er} \text{ OFF} \tag{4.10}$$

$$\dot{x} = A_2 x + B_2 V_{dc} \quad \text{for} \quad Sw_m \text{ OFF}, Sw_1 \text{ ON and } D_{er} \text{ OFF} \tag{4.11}$$

$$\dot{x} = A_3 x + B_3 V_{dc} \quad \text{for} \quad Sw_m \text{ OFF}, Sw_1 \text{ OFF and } D_{er} \text{ ON} \tag{4.12}$$

where

$$A_1 = \begin{bmatrix} -1/(R+esr)C & 0 \\ 0 & -r_{L1}/L_1 \end{bmatrix}, \quad A_3 = \begin{bmatrix} -1/(R+r_c)C & 0 \\ 0 & -\rho/L_2 \end{bmatrix},$$

$$A_2 = \begin{bmatrix} -1/(R+r_c)C & R/(R+r_c)N_1C \\ -\dfrac{N_1}{L_1}\left(1-\dfrac{r_c}{R+r_c}\right) & (-)\left\{\dfrac{r_{L1}}{L_1}+\dfrac{r_c}{L_1(R+r_c)}\right\} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 \\ N_1/L_1 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \quad B_3 = \begin{bmatrix} 0 \\ -N_2/L_2 \end{bmatrix}$$

These matrices are derived by forming the state equation from the equivalent circuit of Fig. 4.4. The details are given in Appendix A.1.

The converter has been operated at various duty cycles and the steady state waveforms are recorded on an oscilloscope. The experimental waveforms are compared with simulation result at similar conditions. It has been found that the experimental and simulation results are quite close. We have presented two set of simulation and experimental results here. Figs. 4.10 to 4.13 show the simulation results while Figs. 4.14 and Fig. 4.15 depict oscillograms.

The simulation and experimentation has been done for the following conditions. The converter is operated at 26.3 kHz with a supply voltage of 20V. The main switch has duty ratio of 0.58 and load switch is operated at a duty ratio of 0.37. The simulation results are shown in Figs. 4.10 and 4.11.

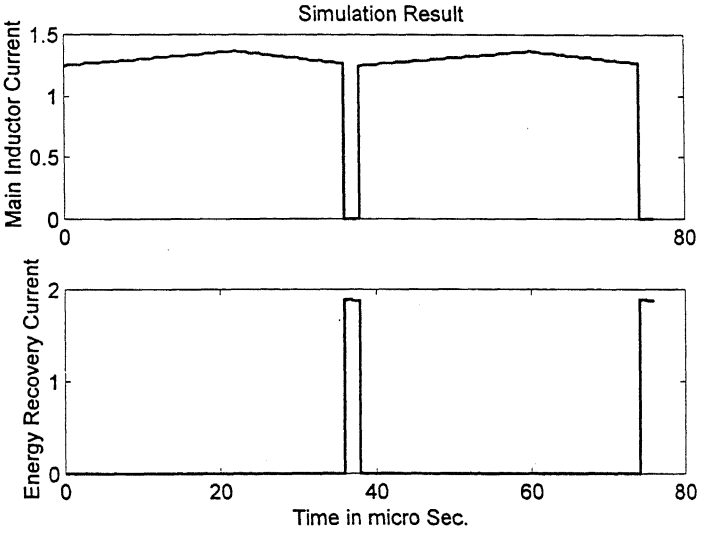


Fig. 4.10 Simulated (a) Main Inductor current and (b) Energy recovery Current

The output voltage as per the simulation study is 23.8 V. The experimental result corresponding to these conditions is shown in Fig. 4.14 where the measured output voltage is 17.8 V. For an ideal converter running at said duty ratios the calculated value of the output voltage from (4.2) is 27.285 V. The value of the output voltage as per the averaging theorem is larger since the ideal converter equation does not account for the actual circuit parameters such as resistance of the windings, their leakage inductance and other

parameters. Similarly, the simulation study has been carried out with assumption of zero leakage inductance and hence it also gives us output voltage larger than experimental value. The simulation and experimental results at other duty ratio shows similar behavior and hence not included here.

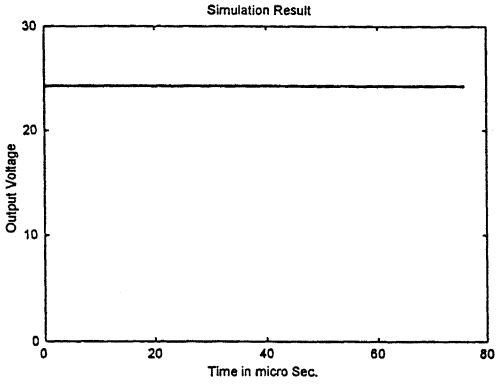


Fig. 4.11 Simulated Output Voltage

The converter is operated at 48.66kHz i.e. at a higher frequency than the previous condition. The main and load duty ratios are respectively 0.4 and 0.3 and load resistance is 18Ω. The simulation results are shown in Figs. 4.12 and 4.13, and corresponding experimental result is given in Fig. 4.15. The ripple contents of the core mmf have substantially reduced compared to the ripple contents at lower frequency. It can be seen from these figures that the experimental and simulation results have a close match.

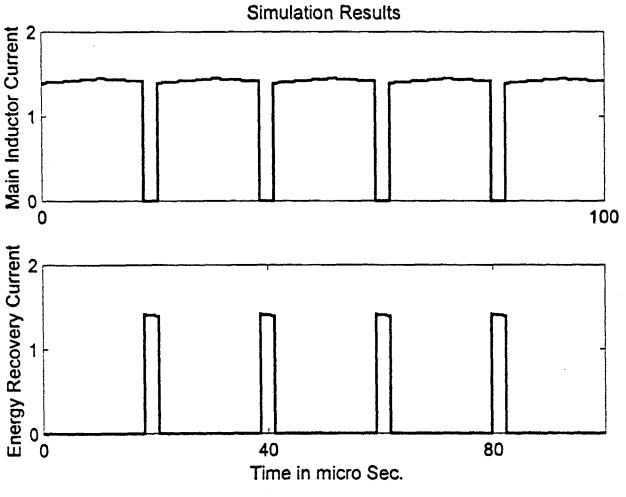


Fig. 4.12 Simulated (a) Main Inductor current and (b) Energy recovery Current

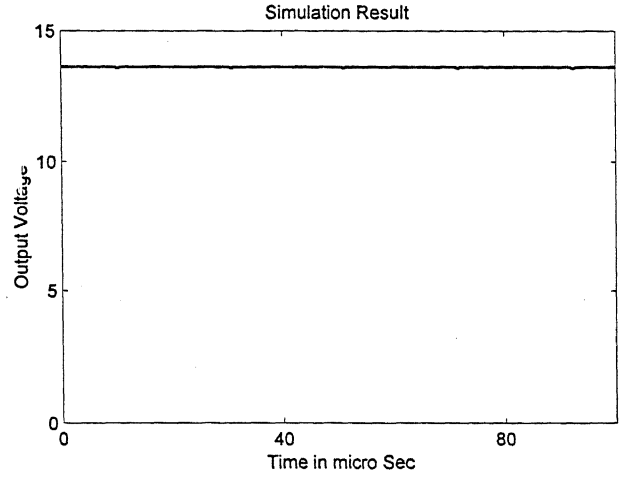


Fig. 4.13 Simulated Output Voltage

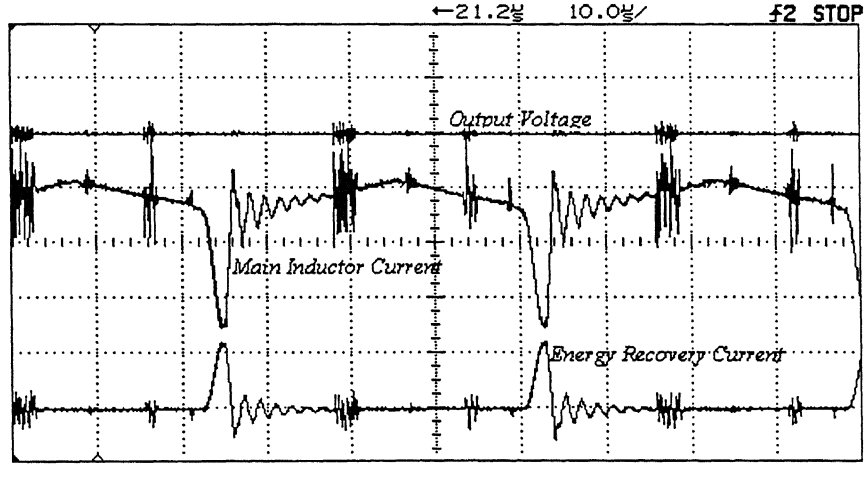


Fig. 4.14 Experimental waveforms observed on oscilloscope for a single output modified Buck-Boost converter operating at 26KHz.

It is to be noted that the experimental waveforms show a very high frequency oscillation of the 10 MHz range in both inductor charging and capacitor charging intervals. It can be seen from Figs. 4.14 and Fig. 4.15 that these high frequency oscillations exist in energy recovery waveform as well as in the output voltage. These oscillations were also observed on ground even when the power circuit was turned off. It is therefore understood that these high frequency oscillations are either pick up of the oscilloscope's probe or common mode noise.

There are relatively lower order frequency oscillations at turn on of main switch.

These oscillations are due to oscillation between stray capacitance and leakage inductance between main and energy recovery winding. Due to leakage inductance the rate of rise of energy recovery current is also limited. It can be seen that even though the simulation results are very close to the experimental results, there shape and values do not match exactly with the experimental ones. This is due to the fact that simulation does not take in account of the leakage inductance between main and energy recovery windings.

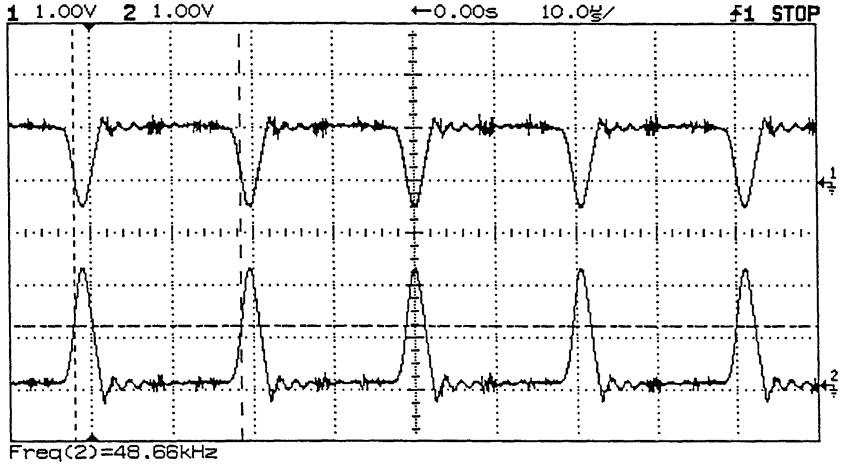


Fig. 4.15 Experimental waveforms for a single output modified Buck-Boost converter at 48KHz showing variation of the Main switch current and energy recovery current over a switching cycle.

In [58] one output is operated in Continuous Conduction Mode (CCM) and the other output in Discontinuous Conduction Mode (DCM) to regulate load perturbations in a dual converter. However the uncontrolled charging of the capacitors do not allow independent regulation of the outputs and the response time is a strong function of the system parameters and the switching frequency. The problem of uncontrolled charging has been solved in [56] for a single output DC-DC converter. The conventional flyback converter has a diode for each output. A switch to obtain better control has replaced the diode in this topology.

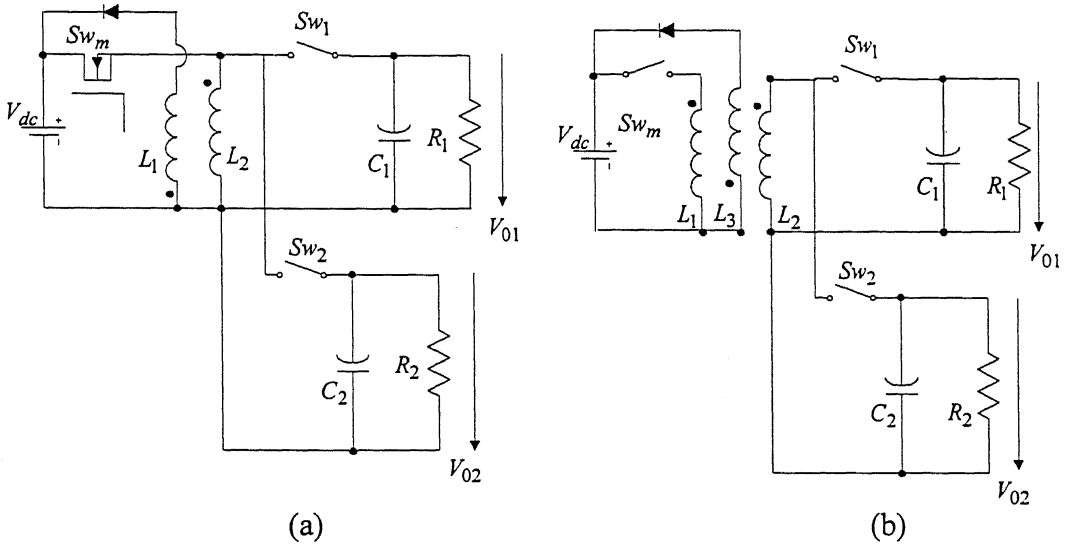


Fig. 4.16 Proposed converter in two-topology: (a) non Isolated (b) isolated Multiple output flyback converters

A new multiple-output topology that has a faster dynamic response is proposed here. This is an extension of the topology given in Fig. 4.1. In the proposed converter, shown in Fig. 4.16, each of the two outputs can be individually controlled between specified minimum and maximum instantaneous values. An energy recovery winding has been used to facilitate opening of all switches whenever required. If we call load switch along with capacitor and load as load sub-circuit, additional load sub-circuits will realize a converter topology with increased numbers of outputs. Fig.4.16 (a) can be called non-isolated topology as the flyback inductor is common to input and output, whereas Fig.4.16 (b) can be termed as an isolated topology for two output converter.

4.5.1 Steady State Analysis

The steady state operation of the converter in constant frequency has been shown by switching diagram in Fig. 4.17. The switching diagram is drawn for two outputs. The main switch that builds flux in the core is used in sequence by two load circuits in intervals d_1T and d_2T respectively to charge the output capacitors. This may be followed by an energy recovery interval $d_{er}T$ if required. However, the energy recovery period can be positioned in any place in a switching period T. The average output voltages is not a function of the energy recovery position as can be seen from (4.13). The isolated version of the converter topology also has almost the same switching diagram. The output voltage governs the turn ratio of the main transformer. The equivalent circuit diagrams for different switching intervals are shown in Fig. 4.18.

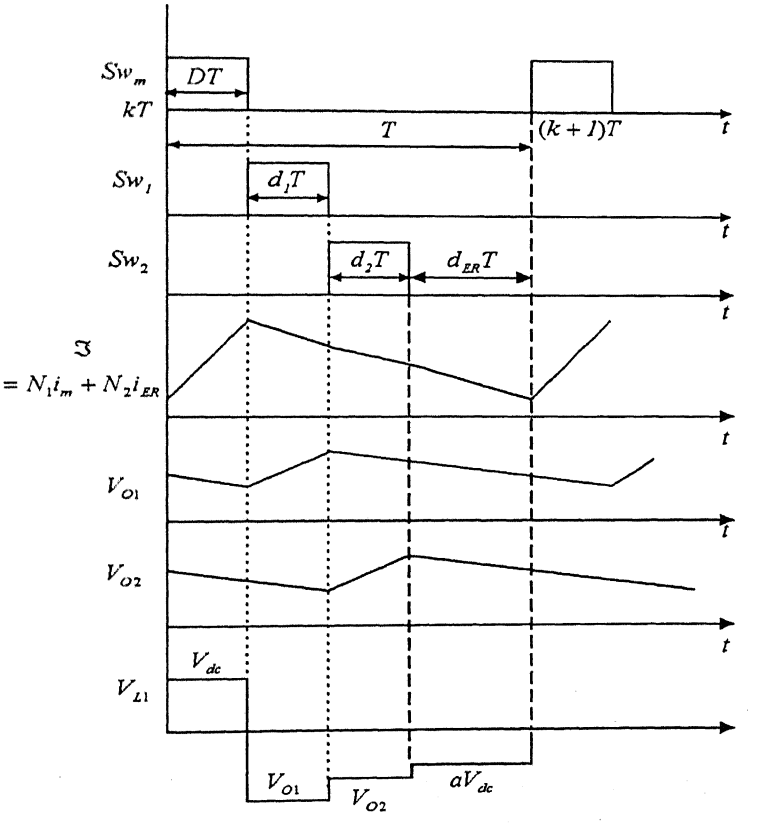


Fig. 4.17 Switching diagram for multiple output converter

The inductor-charging interval DT starts with closing of main switch and opening of load switches Sw_1 and Sw_2. The equivalent circuit is shown in Fig. 4.18 (a). This

interval followed by opening of the main switch Sw_m and closing of load switch Sw_1 (equivalent circuit given in Fig. 4.18 b). Next the load switch Sw_2 is closed and the switch Sw_1 is opened (equivalent circuit given in Fig. 4.18 c). Fig. 4.18 (d) shows the equivalent circuit of the optional energy recovery interval, where all the switches are open.

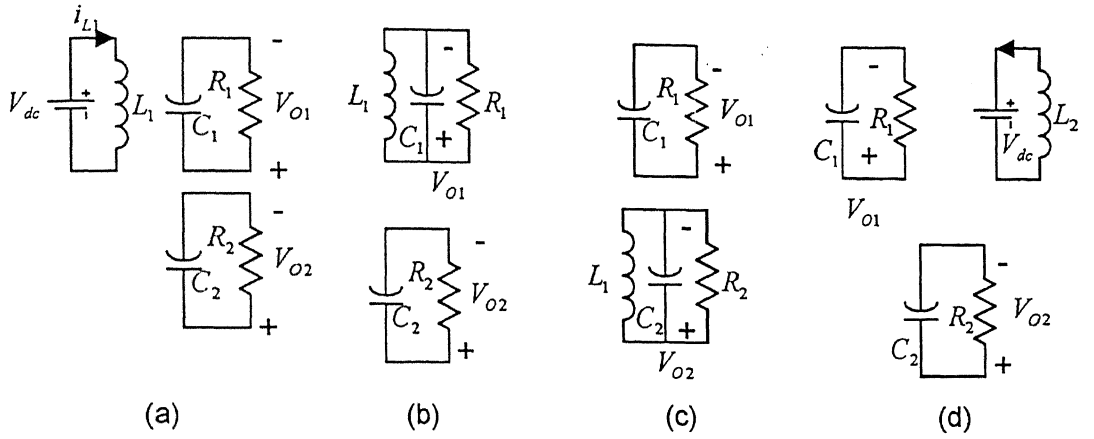


Fig. 4.18 Equivalent circuits of multiple output converter for (a) main Switch conducting (b) load Switch 1 conducting (c) load switch 2 conducting and (d) Energy recovery operating

The expression for output voltages are obtained by voltage-second balance of the core and charge balance across capacitors. The resulting equations are given by

$$\left.\begin{aligned}\frac{V_{O1}}{V_{dc}} &= \frac{D - a\,d_{er}}{d_1\left[1+\left(\frac{d_2}{d_1}\right)^2\frac{R_2}{R_1}\right]}\\ \frac{V_{O2}}{V_{dc}} &= \frac{D - a\,d_{er}}{d_2\left[1+\left(\frac{d_1}{d_2}\right)^2\frac{R_1}{R_2}\right]}\end{aligned}\right\} \qquad (4.13)$$

It is to be noted here that the converter steady state characteristic given by (4.13) is for constant frequency duty programmed converter operation. The steady state characteristics of two output modified converter have been plotted in Fig. 4.19 to Fig. 4.22. It can be easily be seen from (4.13) that there exist cross-correlation between the outputs. Changing the duty and turns ratios of any one of the converters affects the output of the

other. This goes against the heuristic search of a converter topology for independent output voltage regulation. Due to the cross regulation at constant frequency operation, the converter has been analyzed in steady state and verified experimentally in open loop only.. It will be shown in Chapter 5 that this converter will be able to contain the cross regulation with a hysteresis controller.

The voltage gain of each of the outputs of the two-Output converter is a function of main duty, load duties, turns ratio and ratio of the load resistance. It can be seen from Figs. 4.19 to 4.20 that the change in loading factor (R_1 / R_2) changes the voltage gain and zone of CCM operation. The peak voltage gain of the output-1 changes from 1.25 at $(R_1 / R_2) = 1.1$ to 3.75 for a ratio $(R_1 / R_2) = 5$. The rate of rise shown in Fig. 4.19 is smoother than to that of Fig. 4.20. The rate of voltage rise with duty is thus a function of resistance ratio. The converter outputs are capable of working in both buck and boost modes.

Fig. 4.21 shows the cross regulation of the outputs. A change in the load duty of output-1 when the load duty of output-2 is held constant changes the voltage gain of output-2. In the similar way it can be shown that the output-1 changes with change in load duty of switch 2. The cross regulation effect forces output 1 to be in buck mode only as shown in Fig. 4.22. Therefore, constant frequency operation of multiple output converter does not serve the purpose of faster response and minimum cross regulation.

4.6 SMALL SIGNAL MODELING OF SINGLE OUTPUT MODIFIED DC-DC CONVERTER

The single output modified Buck-Boost converter of Fig. 4.1 has three independent subintervals, namely main switch ON interval, load switch ON subinterval and energy recovery interval. The main and load duty ratio is independently controllable. The state space equations for the converter in different intervals of the converter operation have been given in equation (4.10) to (4.12). The small signal model for a multiple sub-interval has been derived in Section 2.5 of chapter 2 and it is given by

$$\tilde{x}(t_n) = \prod_{i=1}^{n}[\Phi_i']\tilde{x}(t_0) + \left[\prod_{i=1}^{n}\Phi_i' - \prod_{i=1}^{n}\Phi_i\right]x(t_0) + \sum_{j=1}^{n}\left(\prod_{j=1}^{n-j}\Phi_i'\Theta_j' - \prod_{j=1}^{n-j}\Phi_i\Theta_j\right)V_{dc} \qquad (4.14)$$

Using this equation linear and bilinear STM based models will be derived.

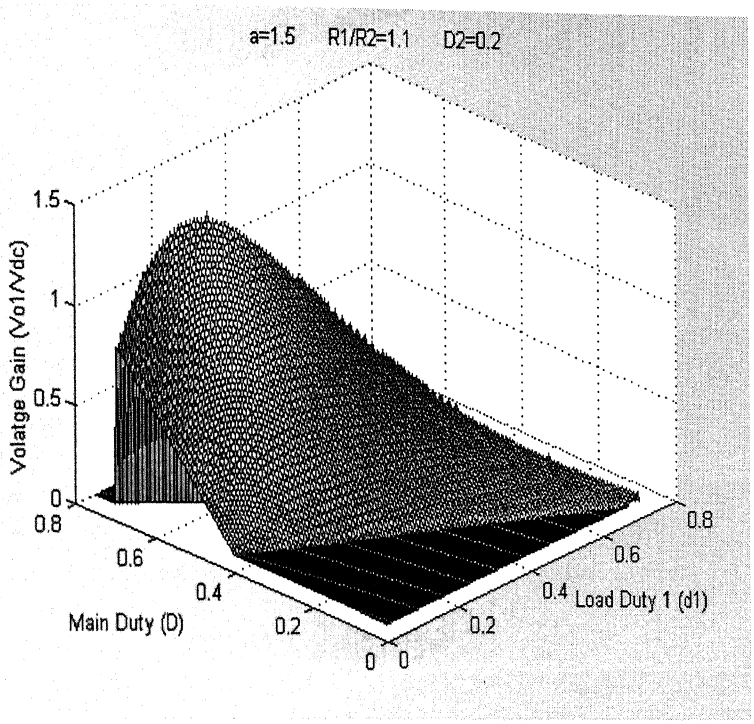


Fig. 4.19 Steady state characteristics of two output converter. Load duty ratio of load switch 2 is held constant at 0.2 at a resistance ratio of 1.1.

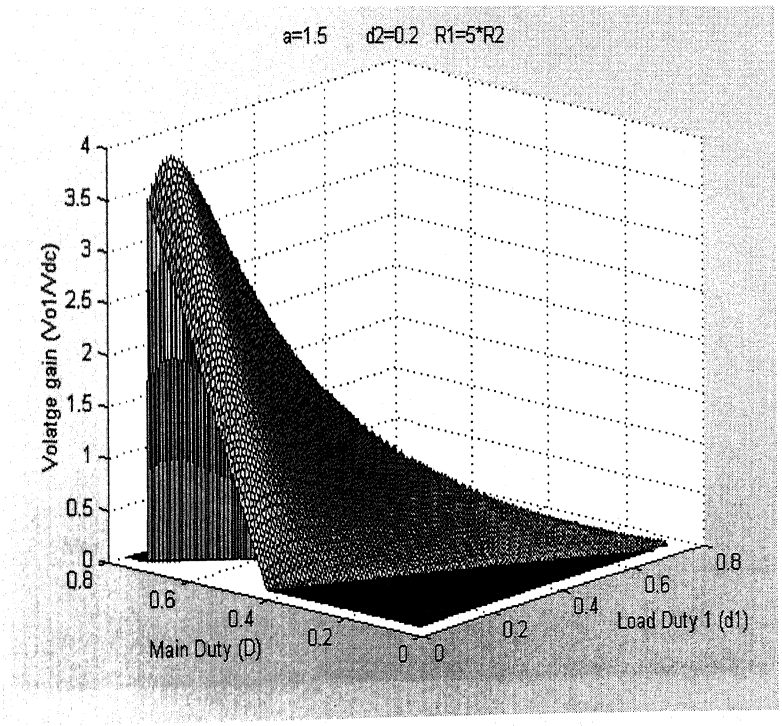


Fig. 4.20 Steady state characteristics of two output converter. Load duty ratio of load switch 2 is held constant at 0.2 at resistance ratio of 5.

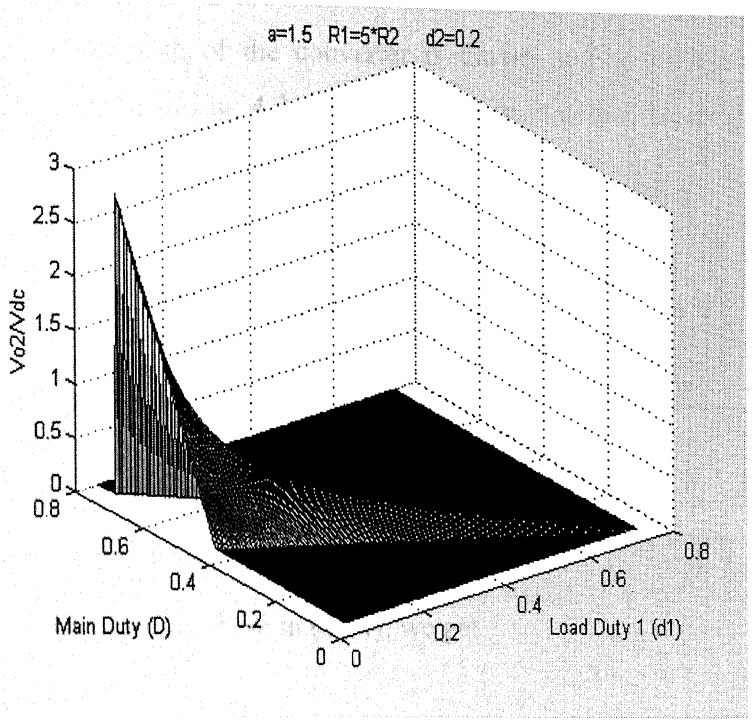


Fig. 4.21 Steady state characteristics of two output converter. Load duty ratio of load switch 2 is held constant at 0.2 at resistance ratio of 5.

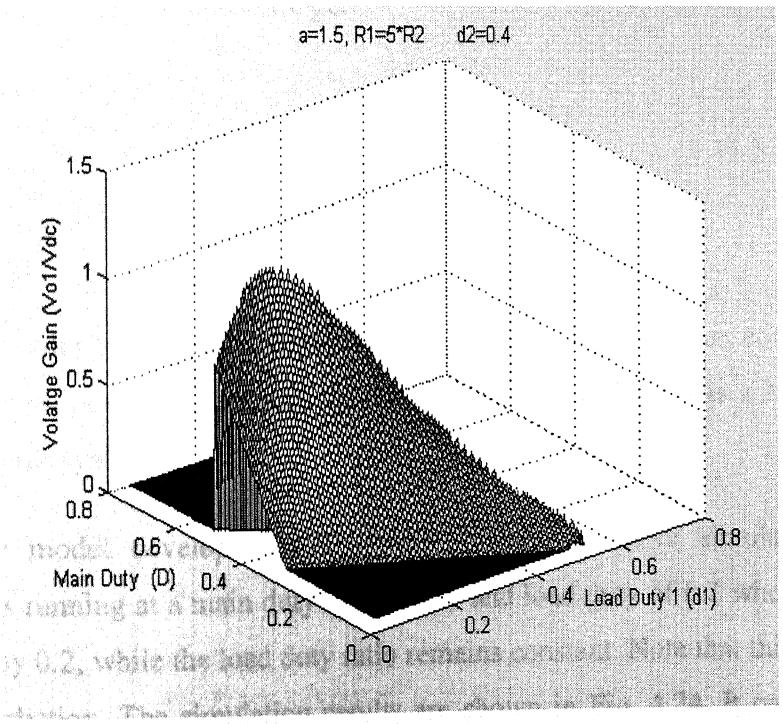


Fig. 4.22 Steady state characteristics of two output converter. Load duty ratio of load switch 2 is held constant at 0.4 at resistance ratio of 5.

4.6.1 Linear STM Based Small Signal Model

The timing diagram of the converter is drawn in Fig. 4.23 on the basis of the switching diagram given in Fig. 4.2. The switching instants and interval lengths are given along with the state matrices in these subintervals.

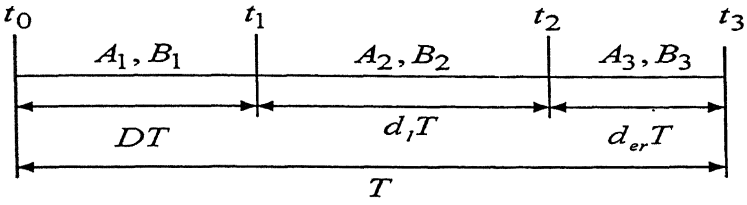


Fig. 4.23 Timing diagram of the converter

Let the state transition matrices in the intervals DT, dT and $d_{er}T$ be Φ_1, Φ_2 and Φ_3 respectively. Substituting these in (4.14), we get

$$\tilde{x}(t_3) = \prod_{i=1}^{3}[\Phi_i']\tilde{x}(t_0) + \left[\prod_{i=1}^{3}\Phi_i' - \prod_{i=1}^{3}\Phi_i\right]x(t_0) + \sum_{j=1}^{3}\left(\prod_{j=1}^{3-j}\Phi_i'\Theta_j' - \prod_{j=1}^{3-j}\Phi_i\Theta_j\right)V_{dc}$$

Simplifying the above equation we get

$$\begin{aligned}\tilde{x}(t_3) &= \Phi_3\Phi_2\Phi_1\tilde{x}(t_0) \\ &+ \left[\left(\Phi_3\Phi_2A_1\Phi_1 - A_3\Phi_3\Phi_2\Phi_1\right)x(t_0)T_s + \left(\Phi_3\Phi_2\Phi_1B_1 - A_3\Phi_3\Phi_2\Theta_1\right)V_{dc}T_s - \Phi_3B_3V_{dc}T_s\right]\tilde{D} \\ &+ \left[\left(\Phi_3A_2\Phi_2\Phi_1 - A_3\Phi_3\Phi_2\Phi_1\right)x(t_0)T_s + \left(\Phi_3A_2\Phi_2\Theta_1 - A_3\Phi_3\Phi_2\Theta_1\right)V_{dc}T_s - \Phi_3B_3V_{dc}T_s\right]\tilde{d}\end{aligned} \quad (4.15)$$

The higher order terms of the expansion of the series has not been considered. Equation (4.15) is linear perturbation model of the converter. Note that it is a MISO (Multi-Input Single Output) system.

The model developed is validated through extensive simulation studies. The converter is running at a main duty ratio of 0.5 and load duty of 0.2 when the main duty is perturbed by 0.2, while the load duty ratio remains constant. Note that this is a considerably large perturbation. The simulation results are shown in Fig. 4.24. It can be seen that the trajectories of simulated system perturbation and the linear STM based prediction overlap.

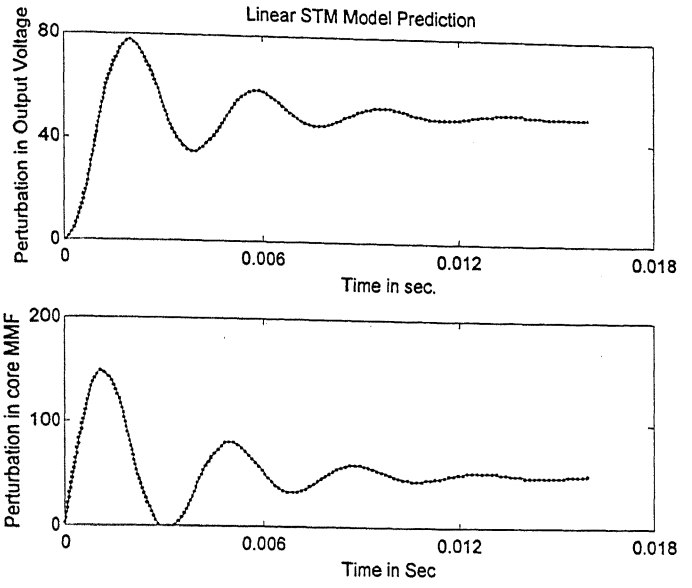


Fig. 4.24 Linear STM based prediction of perturbation of states of the converter.

However, the prediction model, when tested at different operating point, did not succeed as shown in Fig. 4.25. The converter is assumed to be in steady state with a D of 0.6 and d of 0.1. The main duty remains unchanged while load duty is changed by 0.2. It can be seen from Fig. 4.25 that the simulated state dynamics and prediction dynamics do not match at all. The same is true when both main and load duty are changed simultaneously. Thus linear prediction model is not sufficient to model the converter for all operating modes.

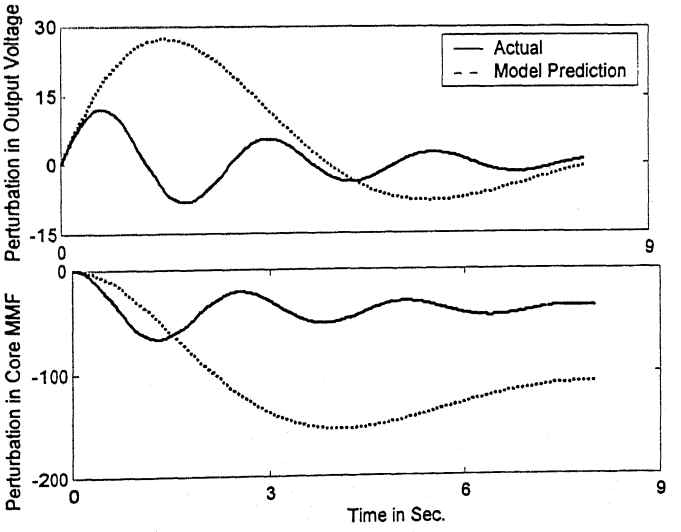


Fig. 4.25 Linear STM based prediction of perturbation of states of the converter.

4.6.2 Bilinear STM Based Small Signal Model

The linear prediction model of the modified buck-boost converter is not capable of predicting the perturbation in states for all possible modes. Hence a bilinear model of the converter has been developed in this section. The bilinear model has been derived from (4.14) by retaining product term of state and duty ratio along with the linear terms of the expansion. The model thus obtained is given as

$$\begin{aligned}\tilde{x}(t_3) = {} & \Phi_3\Phi_2\Phi_1\tilde{x}(t_0) \\ & + \left[(\Phi_3\Phi_2A_1\Phi_1 - A_3\Phi_3\Phi_2\Phi_1)x(t_0)T_s + (\Phi_3\Phi_2\Phi_1B_1 - A_3\Phi_3\Phi_2\Theta_1)V_{dc}T_s - \Phi_3B_3V_{dc}T_s\right]\tilde{D} \\ & + \left[(\Phi_3A_2\Phi_2\Phi_1 - A_3\Phi_3\Phi_2\Phi_1)x(t_0)T_s + (\Phi_3A_2\Phi_2\Theta_1 - A_3\Phi_3\Phi_2\Theta_1)V_{dc}T_s - \Phi_3B_3V_{dc}T_s\right]\tilde{d} \\ & + \left[(\Phi_3\Phi_2A_1\Phi_1 - A_3\Phi_3\Phi_2\Phi_1)T_s\right]\tilde{x}(t_0)\tilde{D} \\ & + \left[(\Phi_3A_2\Phi_2\Phi_1 - A_3\Phi_3\Phi_2\Phi_1)T_s\right]\tilde{x}(t_0)\tilde{d}\end{aligned} \tag{4.16}$$

In order to verify the model, a number of simulations have been carried out. The simulation results are given in Figs. 4.26 to 4.29 and are summarized in Table 4.1. It can be seen that the predicted curve almost matches the simulated curve except in the case of Fig. 4.29. Even in this case the prediction is acceptable.

Table 4.1 Summary of bilinear prediction results

Steady state main duty (D_0)	Steady state load duty (d_0)	Perturbation in main duty ($\tilde{D}$)	Perturbation in main duty ($\tilde{d}$)	Results shown in figure
0.6	0.1	0	0.2	Fig. 4.26
0.5	0.1	0.2	0	Fig. 4.27
0.4	0.4	0.4	- 0.3	Fig. 4.28
0.2	0.75	0.6	- 0.65	Fig. 4.29

The perturbation model of multiple output converters will be too complex as the number of variables is equal to number of outputs plus one. Thus, the model will have ten terms in the bilinear model. Since the steady state performance of the converter in steady state is not satisfactory, small signal modeling has not been carried out.

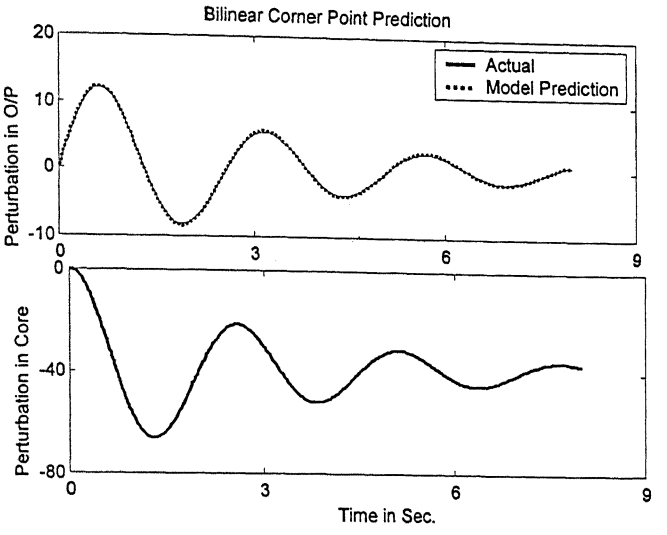


Fig. 4.26 Bilinear prediction for $D_0 = 0.6, d_0 = 0.1, \widetilde{D} = 0, \widetilde{d} = 0.2$

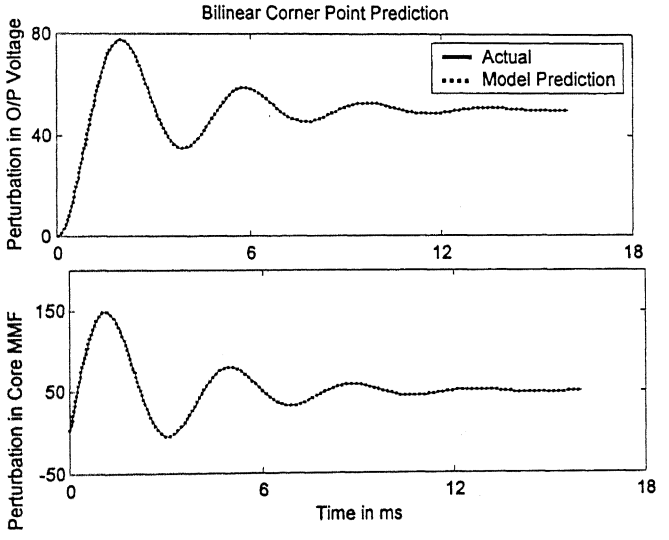


Fig. 4.27 Bilinear prediction for $D_0 = 0.5, d_0 = 0.1, \widetilde{D} = 0.2, \widetilde{d} = 0$

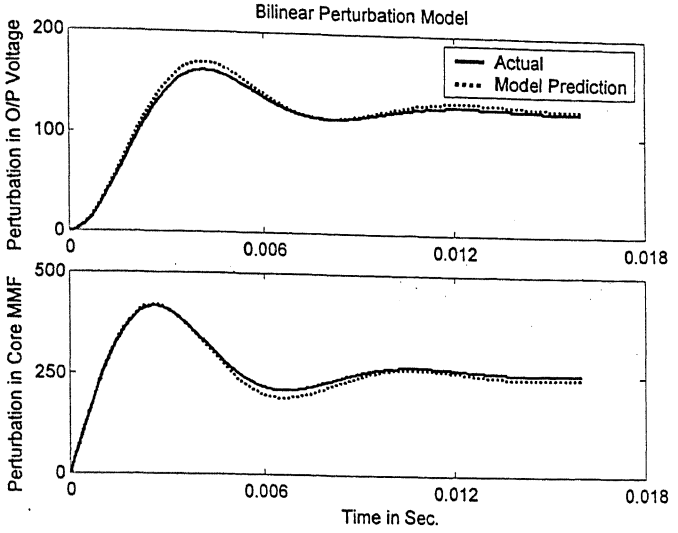


Fig. 4.28 Bilinear prediction for $D_0 = 0.4, d_0 = 0.4, \tilde{D} = 0.4, \tilde{d} = -0.3$

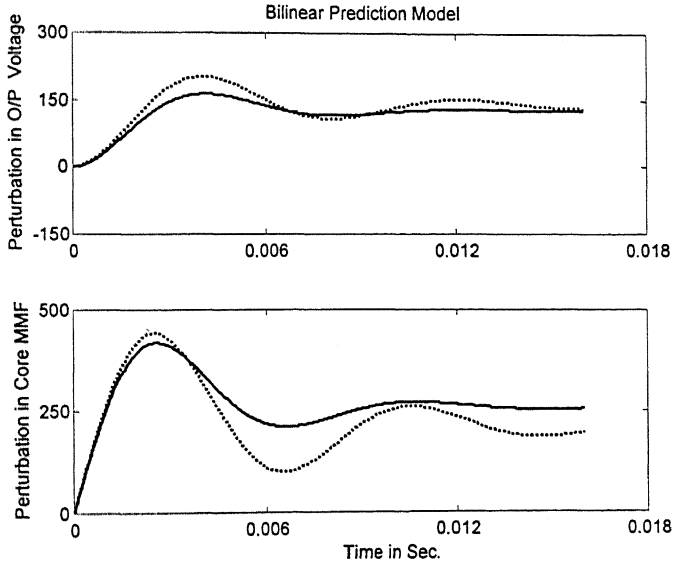


Fig. 4.29 Bilinear prediction for $D_0 = 0.2, d_0 = 0.75, \tilde{D} = 0.6, \tilde{d} = -0.65$

4.7 CONCLUSIONS

A novel converter topology called modified buck-boost converter has been proposed. The independent charging of core mmf and output capacitor is made possible. The converter has been characterized in steady state for constant frequency CCM operation. The modified converter characteristics in constant frequency operation are comparable with

its conventional counterpart buck-boost converter. The modified buck-boost converter topology has further been extended for multiple output. This converter has also been characterized for constant frequency in CCM mode. These converters are assumed to be duty programmed, i.e. the control input of the converter is duty ratio. The characteristics discussed shows marginal improvement over the conventional converter. The steady state characterization suggests for a non-duty-programmed mode of operation to utilize the additional facility of opening the load switch.

The small signal modeling for constant frequency operation of converter in CCM mode has been done. The perturbation model requires bilinear terms to take in account of possible perturbations of the converter inputs. The bilinear model is therefore minimum order model of the proposed converter.

CHAPTER 5

HYSTERESIS CONTROL OF MODIFIED CONVERTER

In Chapter 4, we have seen that the modified Buck-Boost converter operating in constant frequency requires a bilinear model to describe small signal perturbation. Thus, designing a closed loop controller using method discussed in chapter 3 is highly complicated and computationally extensive. Therefore, an alternate control strategy for modified Buck-Boost converter called hysteresis controller has been suggested in this chapter. This not only simplifies the closed loop controller design but also simple to fabricate in hardware. A new closed loop controller called hysteresis controller has been proposed in this chapter. Extensive simulation and experiments have verified the proposed closed loop hysteresis controller. The proposed closed loop control scheme is simple in hardware realization and performs very well.

5.1 HYSTERESIS CONTROL OF MODIFIED BUCK-BOOST CONVERTER

In this section, we introduce the concept of the hysteresis controller to be used for closed loop operation of modified converters. Next, a conceptual design of the hysteresis controller for single output modified Buck-Boost converter has been carried out.

5.1.1 An Introduction to Hysteresis Control

The prime objective of a closed loop controller for a DC-DC converter is to reject input and load disturbances without losing stability. Improvements in response time, extension of zone of validation, etc. are some of other possible secondary objectives of closed loop controllers. But a better dynamic performance is essential for critical loads.

A DC-DC converter is controlled by changing the duty ratio. Other methods are derived methods of duty ratio control to achieve a better control than direct control of duty. One such method is known as current programmed converter. The current programmed closed loop control has been widely studied in the literature. Inclusion of feed-forward loop in closed loop controller has been suggested to improve dynamic response. It is possible to compensate the supply disturbance in one cycle as reported in [54].

An attempt to compensate the load side disturbance of a conventional Buck-Boost converter in minimum time by [54] will not succeed because of indirect control of the load circuit. By load circuit we mean series combination of diode with the parallel load resistance and output capacitor. Note that the load circuit of conventional Buck-Boost converter gets connected to inductor when the switch turns OFF. Therefore we have proposed modified topology in chapter 4. The small signal model of this converter is bilinear in both duty ratios with the state of the converter. Thus, the closed loop controller design will be highly complicated. Therefore hysteresis controller has been proposed in this chapter.

Although the theory of hysteresis control is well established, this is repeated here for sake of continuity. A variable(s) to be controlled is identified in a given circuit. The desired closed loop state trajectory is described for the variable. The feasibility study and stability requirements of the closed loop trajectory are made by suitable control theorems. This trajectory is now set as the reference value for the variable. We form a band called hysteresis band around this reference. The circuit is switched in such a manner that the actual state trajectory never goes out of this band. The average states of the converter therefore follow the set reference with high frequency component due to switching. This method of closed loop is called hysteresis control.

The operation of the converter is as follows. The core mmf builds when the main switch of the converter is closed. The stored magnetic energy is then used for charging load circuit. If the core energy is more than the energy required for load circuit in a switching cycle, the excess energy is fed back to the input by energy recovery circuit. In case the load rejection takes place in the circuit, the amount of the excess energy goes up and thus the energy recovery interval is proportionately increased. However, if the energy demand of the load goes up, there is no solution but to wait for the magnetic energy to build up. This will make the dynamic response slow. Had there been some excess energy available when required by the load, the compensation could have been done instantaneously. Keeping this in view, the closed loop controller has been designed. The reference core energy is chosen to account for maximum loading condition. If the loading is less, the energy recovery is more and if the loading is at its peak, there is no energy recovery. The output voltage starts dropping for loads more then the designed maximum load. This is also known as folding characteristics of the converter. The operation of the hysteresis controller for single output modified Buck-Boost converter is described in next section.

5.1.2 Operation of Hysteresis Controller

The block diagram of the proposed hysteresis controller is shown in Fig. 5.1. The instantaneous values of core mmf $\Im$ and v_0 are obtained from the converter circuit with the help of suitable transducers. These values are then compared with their respective reference values. The reference value of the output voltage is the desired output voltage and the hysteresis band is equal to the allowed ripple in the output voltage. For the simulation purpose the ripple is assumed to be 5% of the average value.

The determination of reference value of the core mmf for a given load and output voltage is done as follows. Let the core mmf be operated with hysteresis band of $\Delta\Im$ around an average core mmf of $\Im_{av}$. This means that the core mmf has a maximum value $\Im_{\max} = \Im_{av} + \Delta\Im$ and a minimum value of $\Im_{min} = \Im_{av} - \Delta\Im$. Let the main switch Sw_m (Fig. 4.1) be ON for a period of t_{on} and OFF for a period of t_{off}. For negligible energy recovery interval the turn ON and turn OFF periods are given by (5.1).

$$t_{on} = \frac{\Delta\Im}{N_1 V_{dc}} L_1 \qquad \& \qquad t_{off} \approx \frac{\Delta\Im}{N_1 V_o} L_1 \tag{5.1}$$

Let $T = t_{on} + t_{off}$ be the switching period of the main switch Sw_m. It is given by,

$$T = t_{on} + t_{off} = \frac{\Delta\Im}{N_1 V_{dc}} L_1 \left[1 + \frac{V_{dc}}{V_o} \right] \tag{5.2}$$

The average value of the core mmf for a variable frequency operation of the converter is obtained from (4.3a) and is given by,

$$F_{av} = N_1 \left(\frac{T}{t_{off}} \right) \left(\frac{V_0}{R} \right) \tag{5.3}$$

Solving (5.1),(5.2) and (5.3), we obtain (5.4).

$$F_{av} = \left(\frac{N_1 V_0}{R} \right) \left(1 + \frac{V_0}{V_{dc}} \right) \tag{5.4}$$

The average value of the core mmf obtained in (5.4) serves as the guideline for choosing the reference value of the core mmf. For example if the desired output voltage is 25 V, i.e. $V_0 = 25V$ at an input voltage of 25 V ($V_{dc} = 20V$). If a maximum loading of the $R = 5\Omega$ and number of turns in the inductor is 150, the average core mmf calculated from (5.4) is $F_{av} = 1687.5\ AT$. It is to be noted that this will allow the converter to operate with almost zero ripples in core mmf and output voltage. Since this value is quite large, we perform simulation to obtain minimum possible mmf with acceptable ripple in the output voltage and core mmf. It has been found that if the reference value of the core mmf is 45 to 50 % of the average core mmf calculated from (5.4), the ripple in the output voltage is significantly small and acceptable for all practical purposes.

The hysteresis bandwidth for the core mmf is decided on the basis of the desired frequency of closed loop operation of the converter. Smaller is the hysteresis band higher is frequency of operation of the converter and vice versa. The mmf loop has been given top

priority to protect the main switch from thermal runaway. The voltage loop therefore gets the second priority. As per this control strategy, the gating signal for load switch Sw_1 is derived from gating signal of the main switch Sw_m. It has been said in chapter 4 that the converter may require third switch for certain conditions. If the third switch in place of the diode in the energy recovery winding is used, the logic for gating for this switch will be $Sw_2 = \overline{Sw_m + Sw_1}$.

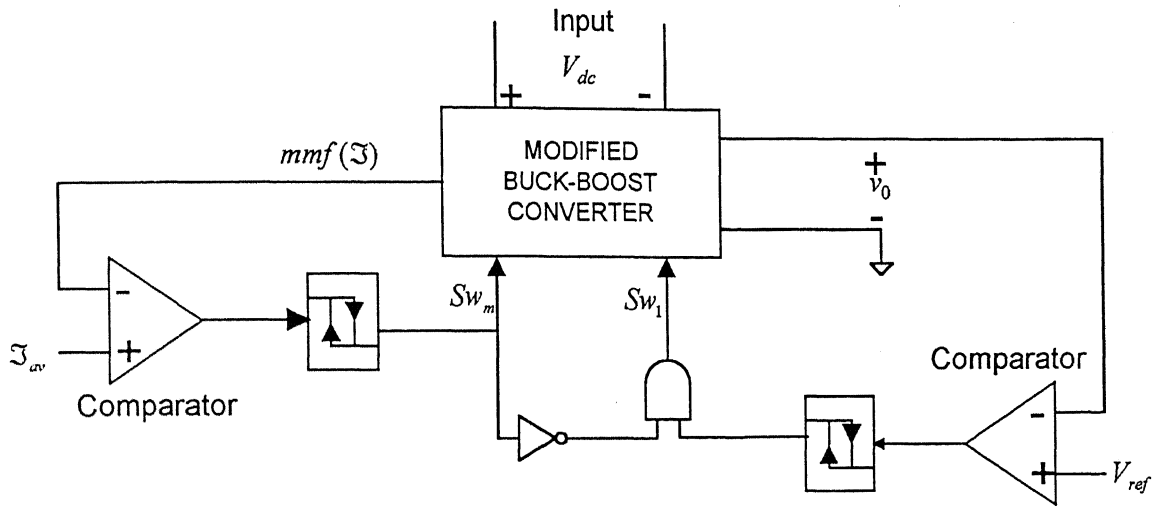


Fig. 5.1 Schematic diagram of the hysteresis controller

The value of load resistance $R = R_c$ for which the energy recovery interval is zero has been called critical resistance. For the specified values of core mmf, voltage limits and converter parameters, the critical resistance can be obtained as follows.

$$\Delta\Im = \Im_{\max} - \Im_{\min} = \frac{N_1 V_{dc}}{L_1} t_{on} \tag{5.5}$$

Solving the dynamic equations of load circuit, we get (5.6)

$$V_{c\min} = V_{c\max} \exp\left(-\frac{t_{on}}{R_c C}\right) \tag{5.6}$$

Eliminating t_{on} by combining (5.1) and (5.6) we get

$$R_c = \frac{\Delta\Im}{\ln\left(\frac{V_{c\max}}{V_{c\min}}\right)} \frac{L_l}{C} \frac{1}{N_l V_{dc}} \tag{5.7}$$

For any value of $R < R_C$, the output voltage will hit the minimum limit of hysteresis band of voltage V_{cmin} before the core mmf has reached its peak value $\Im_{max}$. Since the mmf loop has top priority, Sw_1 can not turn ON and hence the output voltage keeps falling below the minimum limit V_{cmin} every cycle and thereby, it provides the folding characteristics.

For any value of R greater than R_C, the core mmf $\Im$ reaches the upper limit turning OFF main switch Sw_m before v_0 hits the lower limit. The load switch Sw_1 therefore does not turn ON. Due to simultaneous switching off of main and load switches, the energy recovery takes place till output voltage hits the minimum. If the load is too light, the core mmf may go to its minimum value $\Im_{min}$ due to sustained energy recovery operation turning ON main switch again. The load switch is not required turned on every cycle for such loads. The ripple frequencies of core mmf and output voltage in this condition will be different.

The circuit can be started from cold with the hysteresis controller. The hysteresis mmf controller builds core mmf in one cycle and the output voltage builds up in the consecutive cycles. The rate of rise of inductor current is limited by the self-inductance L_l of the main inductor. Alternatively, the current limits can be ramped to obtain a softer start.

5.2 SIMULATION RESULTS FOR SINGLE OUTPUT CONVERTER

Extensive simulation study has been carried out to establish the following.

- Capabilities to work in all possible modes namely in buck and boost modes.
- Faster dynamic response in presence of load and supply disturbances.

The proposed converter is simulated on digital computer using differential equation model of Chapter 4 and software package, MATLAB. The parameters of converter used for simulation study have been given below.

$$L_1 = 3.5mH, C = 330\mu F, R = 15\Omega, V_{dc} = 20V, a = 3/2$$
$$\Im_{av} = 750\,AT, \quad \Delta\Im = 0.1 * \Im_{av}, \Delta V_0 = 0.05 V_0 \; N_1 = 150$$

The simulation parameters given above have been taken from the hardware setup used for experimental verification of the hysteresis controller in section 5.3. The simulation study carried out for single output modified Buck-Boost converter with hysteresis controller in the closed loop is summarized in Tables 5.1 and 5.2. As mentioned earlier, the converter can be operated in buck and boost modes. The buck and boost mode operation with possible disturbance studies are listed in Table 5.1 and Table 5.2 respectively. The simulation studies are carried out assuming that both the switches and inductance are ideal and the measurements made are true without any error or disturbance.

Table 5.1 Buck mode operation of Modified Buck-Boost Converter

V_{dc}	ΔV_{dc}	R	ΔR	$V_{0,ref}$	Result shown in	Comments
Steady State Behavior for Different Operating Points						
20	--	15	--	15	Fig 5.2 (a)	$V_0 / V_{dc} = 0.75$
20	--	15	--	10	Fig 5.2 (b)	$V_0 / V_{dc} = 0.5$
Effect of Load Disturbances						
20	--	15	35	10	Fig. 5.3 (a)	Load Rejection
20	--	15	-10	10	Fig. 5.3 (b)	Step Loading
Effect of Supply Disturbance						
20	10	15	--	10	Fig. 5.4 (a)	Increased Input
20	-10	15	--	10	Fig. 5.4 (b)	Decreased Input
Effect of combined Load and Supply disturbance						
20	10	15	35	10	Fig. 5.5 (a)	Load Rejection with increase in supply voltage
20	-10	15	35	10	Fig. 5.5 (b)	Load Rejection with decrease in supply voltage
20	10	15	-10	10	Fig. 5.6 (a)	Step Loading with increase in supply voltage
20	-10	15	-10	10	Fig. 5.6 (b)	Step Loading with increase in supply voltage

5.2.1 Simulation Results for Buck Mode operation

The converter operation in steady state is analyzed for various gains V_0 / V_{dc} and possible disturbances in load and input voltage. The results are shown in Figs. 5.2 to 5.6.

The steady state operations at different output voltages, namely at 15V and 10V are shown in Fig. 5.2(a) and 5.2(b) respectively. The supply voltage has been taken to be 20V and load resistance to be 15 Ω. The reference core mmf is 750 AT. The ripples are set to be 10 % of their average reference value. The simulation results also include the cold start transient. The core mmf builds up in single stretch while the output voltage builds slowly. The ripples are within the acceptable limits even if the reference core mmf is very small (nearly 45 % of the calculated value).

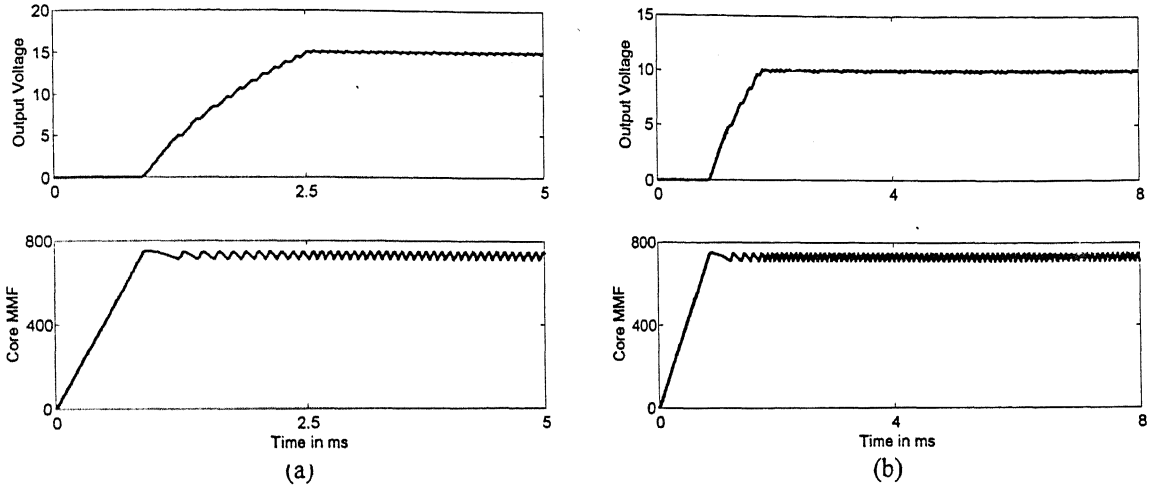


Fig. 5.2 Steady state operation of modified Buck-Boost converter for output of (a) 15V and (b) 10V

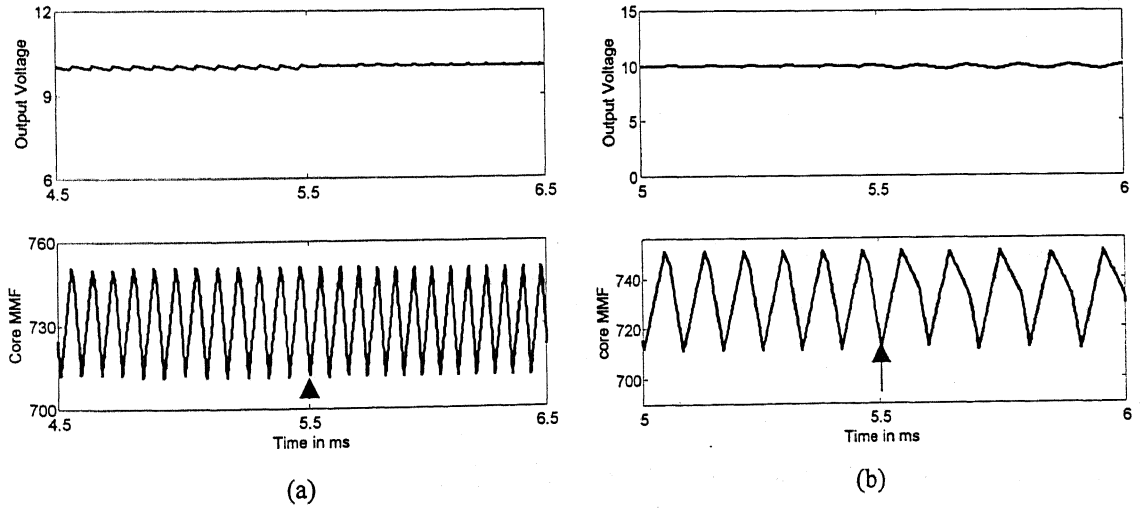


Fig. 5.3 Simulation result for load disturbance (a) Load changed from 15 Ω to 50Ω. (b) Load changed from 15 Ω to 5Ω.

Note that the instant of disturbances is marked by arrowhead line in the figures. The effect of load disturbance on the closed loop performance is shown in Fig. 5.3. The load experiences a step change of 35 Ω in the load resistance changing, i.e. load resistance increases from 15 Ω to 50 Ω. The simulation result for this load rejection is given in Fig. 5.3(a). It can be seen that the average voltage is remaining constant but the ripple contents are altered. However, it is almost within in the specified limits.

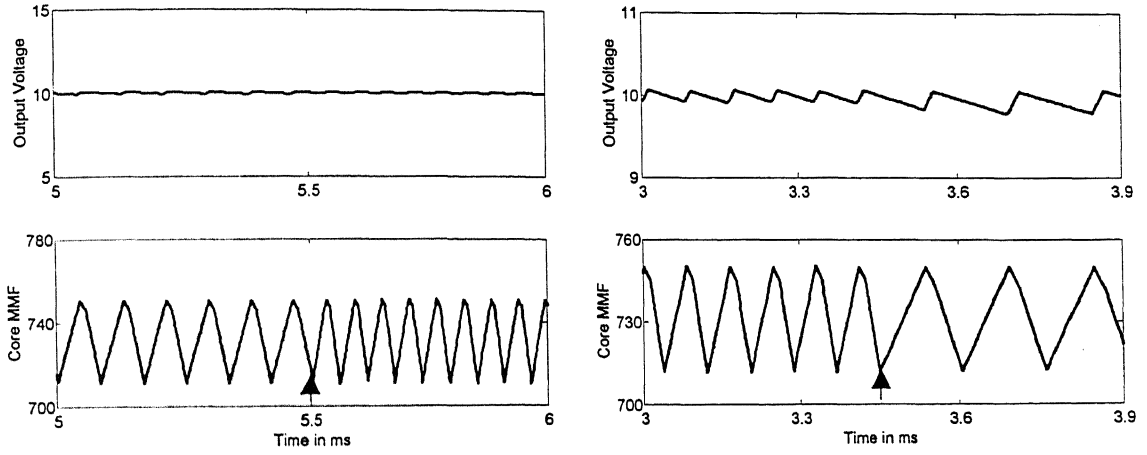


Fig. 5.4 Simulation result for supply disturbance (a) Input Voltage changed from 20V to 30V. (b) Input Voltage changed from 20V to 10V.

The simulation results for evaluation of controller against source disturbances are given in Fig. 5.4. It can be seen that the average voltage remains unchanged whereas the ripple frequency of the core mmf and the output voltage changes. There is slight change in the magnitude of the ripple of the output voltage.

Simultaneous occurrence of load and supply disturbances is simulated and results are shown in Fig. 5.5 and 5.6. Four possible combination of load and source disturbance are simulated in these studies. The effect of load rejection in combination with rise and fall of the supply voltage is given in Fig. 5.5(a) and 5.5(b). Again the average voltage remains unaffected while the ripple contents and the frequency of ripples changed. In the similar

been studied and they have similar a nature and hence are not shown here. The output voltage starts folding if the loading is more than 5Ω. The folding characteristics of the converter with controller for boost mode operation is shown in the following section.

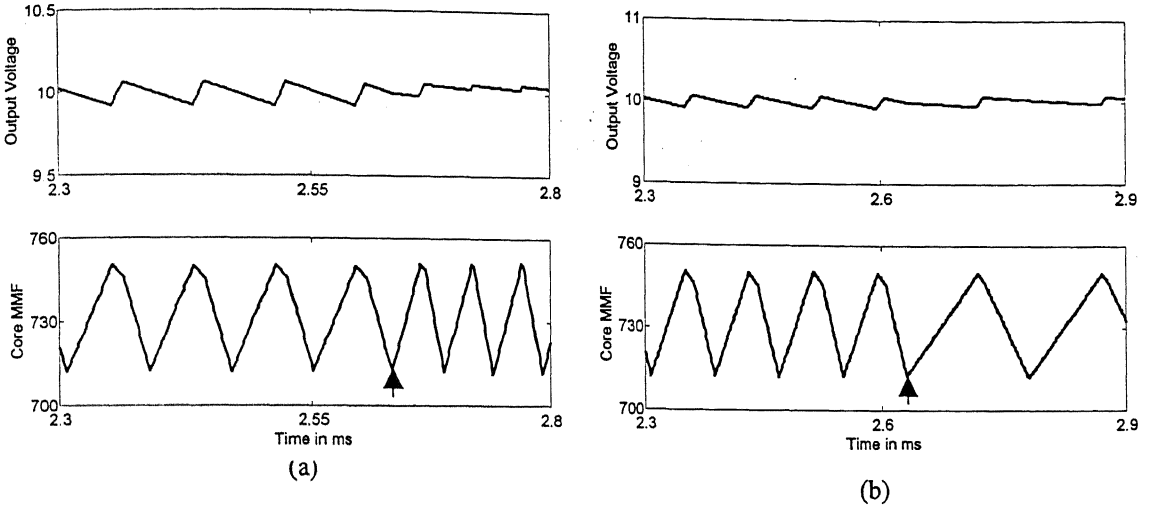


Fig. 5.5 Simulation results for combined load and supply disturbance (a) Input Voltage changed from 20V to 30V.and load changed from 15 Ω to 50Ω. (b) Input Voltage changed from 20V to 10V.and load changed from 15 Ω to 50Ω.

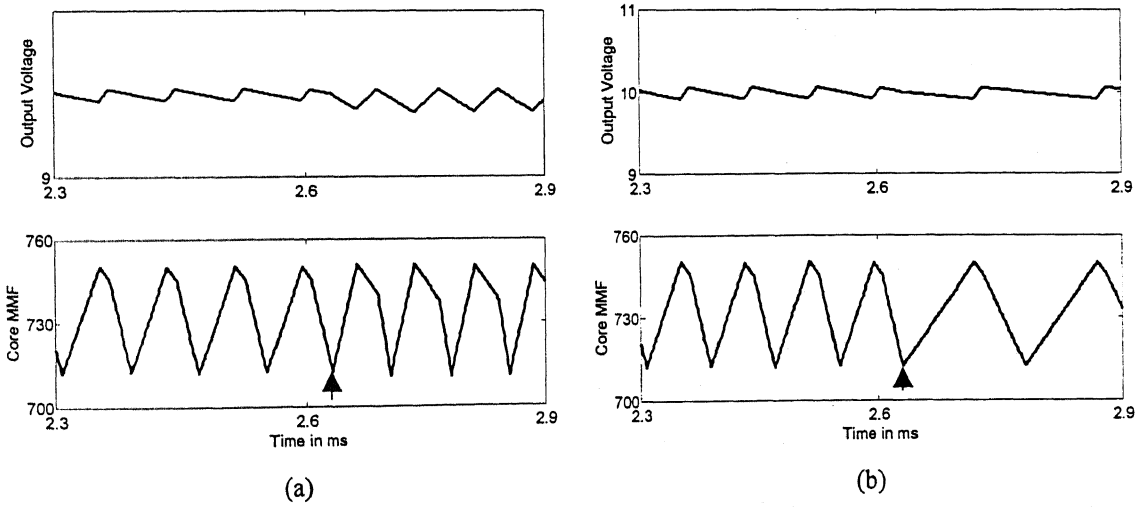


Fig. 5.6 Simulation results for combined load and supply disturbance (a) Input Voltage changed from 20V to 30V.and load changed from 15 Ω to 5Ω. (b) Input Voltage changed from 20V to 10V.and load changed from 15 Ω to 5Ω.

5.2.2 Simulation Results for Boost Mode operation

The converter simulation results in the steady state for various gains V_0 / V_{dc} and closed loop response for disturbances in supply and load are presented in section. The results are shown in Fig. 5.7 to 5.11 and listed in Table 5.2.

Table 5.2 Boost mode operation of Modified Buck-Boost Converter

V_{dc}	ΔV_{dc}	R_L	ΔR_L	V_0	Result shown in	Comments
Steady State Behavior for Different Operating Points						
20	--	15	--	25	Fig 5.7 (a)	$V_0 / V_{dc} = 1.66$
20	--	15	--	30	Fig 5.7 (b)	$V_0 / V_{dc} = 2.0$
Effect of Load Disturbances						
20	--	15	35	25	Fig. 5.8 (a)	Load Rejection
20	--	15	(-)10	25	Fig. 5.8 (b)	Step Loading
Effect of Supply Disturbance						
20	10	15	--	25	Fig. 5.9 (a)	Increased Input
20	(-)10	15	--	25	Fig. 5.9 (b)	Decreased Input
Effect of combined Load and Supply disturbance						
20	10	15	35	25	Fig. 5.10 (a)	Load Rejection with increase in supply voltage
20	(-)10	15	35	25	Fig. 5.10 (b)	Load Rejection with decrease in supply voltage
20	10	15	-10	25	Fig. 5.11 (a)	Step Loading with increase in supply voltage
20	(-)10	15	-10	25	Fig. 5.11 (b)	Step Loading with increase in supply voltage

The converter is simulated for steady state operation in boost mode. The reference core mmf is maintained at 750AT as used in the buck mode operation of the converter. It can be seen from Fig. 5.7(a) that the converter starting from cold is capable of reaching the steady state in relatively large time and the ripple in the output voltage has gone up from 10 % of the average value. But the converter is capable of maintaining the average voltage.

The reference tracking of 30V from the zero state is simulated and the result is shown in Fig. 5.7(b). It can be seen from the figure that the converter is not able to reach this voltage. There remains some steady state error. This is because of the fact that the reference core mmf is 45% of average core mmf calculated from (5.4) for obtaining average

output voltage of 25V. If we increase the reference core mmf the reference voltage can be tracked without error. This simulation therefore shows that the reference voltage tracking is a function of the reference core mmf.

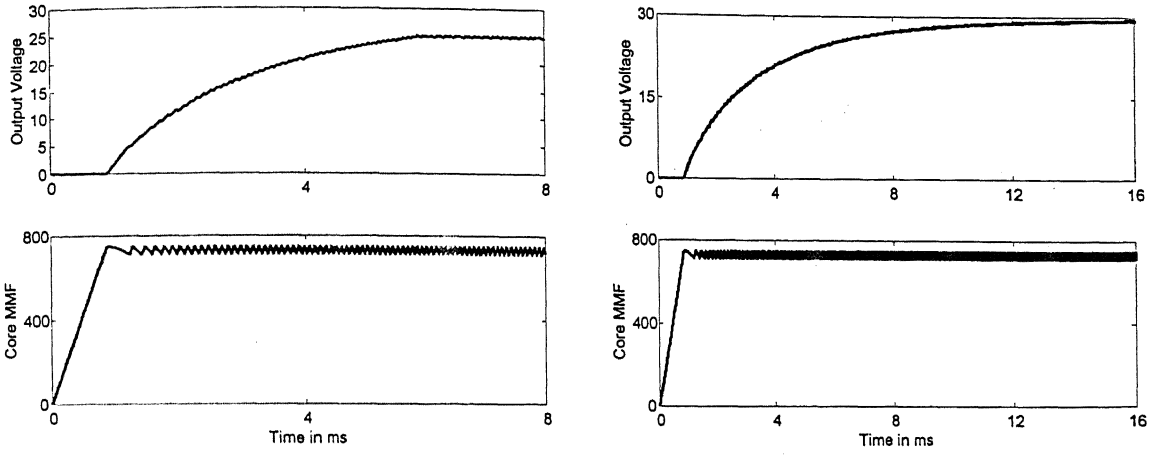


Fig. 5.7 Steady state operation of modified Buck-Boost converter for output of (a) 25V and (b) 30V

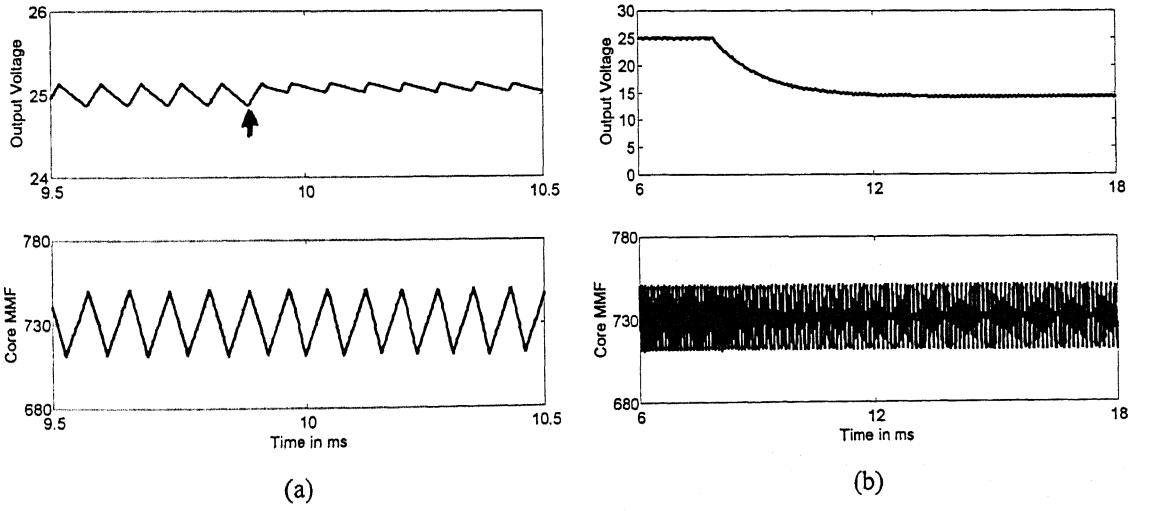


Fig. 5.8 Simulation result for load disturbance (a) Load changed from 15 Ω to 50Ω. (b) Load changed from 15 Ω to 5Ω.

The simulation results shown in Fig. 5.8 are for load disturbance. The load rejection changes the ripple contents of the output voltage and the frequency of the ripples. However, load increase gives the folding characteristics. The output voltage settles around 14.5 V as

shown in Fig. 5.8(b). It is due to the fact that reference core mmf is set 740 AT, which is 45% of the average core mmf, calculated from (5.4) for a loading of 15 Ω at 25V.

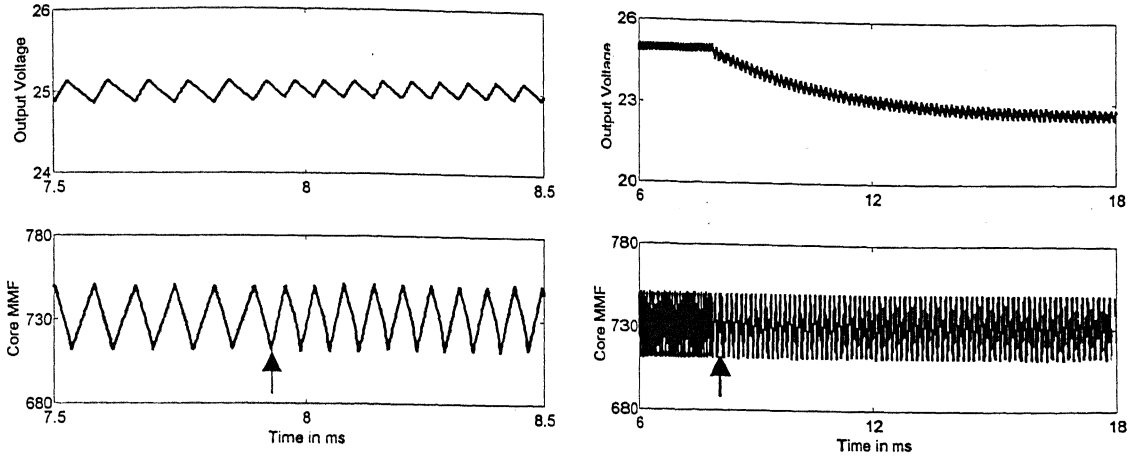


Fig. 5.9 Simulation result for supply disturbance (a) Input Voltage changed from 20V to 30V. (b) Input Voltage changed from 20V to 10V.

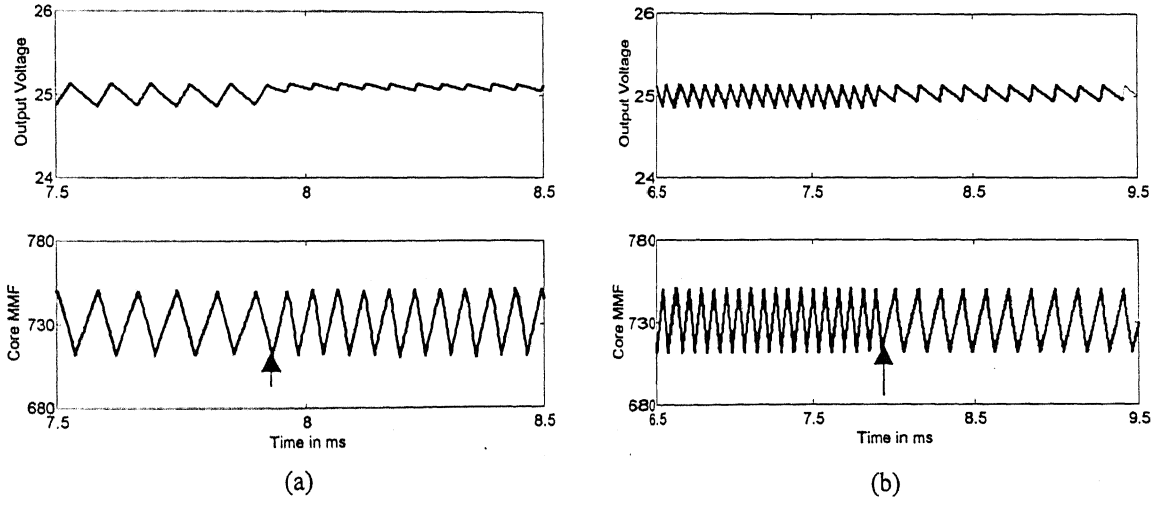


Fig. 5.10 Simulation results for combined load and supply disturbance (a) Input Voltage changed from 20V to 30V.and load changed from 15 Ω to 50Ω. (b) Input Voltage changed from 20V to 10V.and load changed from 15 Ω to 50Ω.

The effect of the positive supply voltage change is similar to that discussed in buck mode operation. The result is shown in Fig. 5.9(a). However, the negative voltage change results in folding characteristics, shown in Fig. 5.9(b). The combined disturbance cases are

shown in Fig. 5.10 and 5.11. Again it has analogous characteristics as to that of the buck mode except the folding characteristics occurring in adverse loading or supply disturbances.

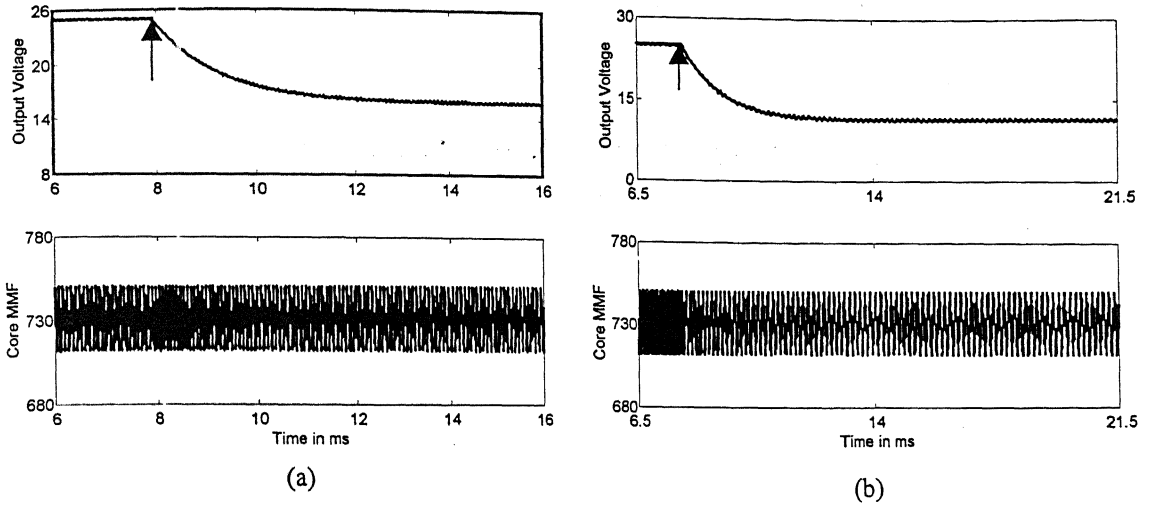


Fig. 5.11 Simulation results for combined load and supply disturbance (a) Input Voltage changed from 20V to 30V.and load changed from 15 Ω to 5Ω. (b) Input Voltage changed from 20V to 10V.and load changed from 15 Ω to 5Ω.

5.3 EXPERIMENTAL RESULTS

An experimental setup has been made in the laboratory to verify the simulation done in the last section. The circuit diagram of the converter is given in Fig. 4.1 and the closed loop hysteresis controller is shown in Fig. 5.1.The details of hardware setup are given in chapter 6. The component values of the hardware setup are given below.

$$L_1 = 3.5mH, \quad C = 330\mu F, \quad a = 3/2, \quad N_1 = 150$$

It is to be noted that the multiplying factor for the output voltage is 4.67 and for the core mmf it is 150 in all the oscillograms.

5.3.1 Experimental Results for Buck Mode

The experimental results shown in this section have been summarized in Table 5.3. The experimental waveform of the converter acquiring steady state operation when started from cold is shown in Fig. 5.12. For this case the desired output is $V_0 = 15$ whereas the

input voltage is $V_{dc} = 20V$ and the load resistance is $R = 150\Omega$. Similarly Fig. 5.13 and Fig. 5.14 shows steady state from cold start for different load and input voltage. These figures show a close resemblance with the simulation results given in section 5.2.1. The detail of the steady state waveform for Fig. 5.13 can be seen in Fig. 5.15.

Table 5.3 Experimental results of converter in Buck Mode

V_{dc}	R_L	ΔR_L	V_0	Result shown in
20	150	--	15	Fig. 5.12
20	10	--	15	Fig. 5.13
30	150	--	15	Fig. 5.14
20	10	--	15	Fig. 5.15
20	150	-140	15	Fig. 5.16
20	10	140	15	Fig. 5.17

In Fig. 5.13, the transient segment shows a dip during its building phase. This may be due to saturation of the core or input dynamics. The waveforms appearing in the oscilloscope for voltage and core mmf shows high frequency noise component. This superimposed noise may be due to various possible reasons, which can be minimized by proper design of the components. The core mmf has relatively higher ripple contents compared to the simulation results. If the high frequency noise is reduced to acceptable limits then the ripple magnitude can further be reduced. Due to these noises when the magnitude is made smaller, it results in malfunctioning of the hysteresis controller causing false triggering of the MOSFET. The frequency of core mmf is also changing due to oscillations occurring at transitions. The approximate frequency of the core mmf is 25KHz. Proper choice of Snubber and minimization of the leakage inductance of the inductance can minimize these problems.

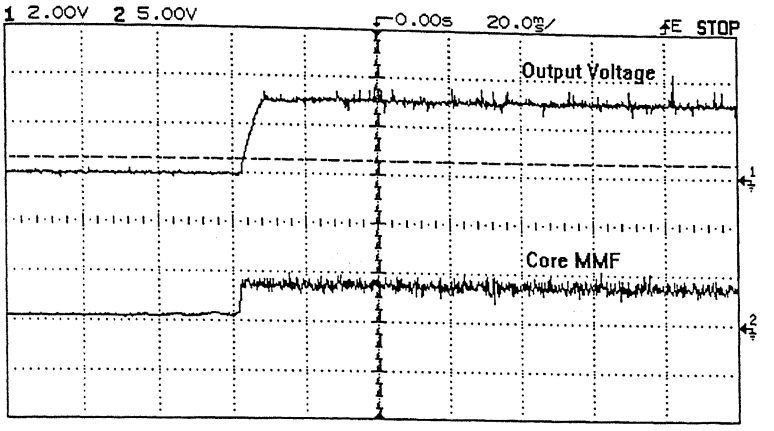


Fig. 5.12 Oscillogram of core mmf and output voltage for output voltage of 15V and input voltage of 20V at a load of 150 Ω.

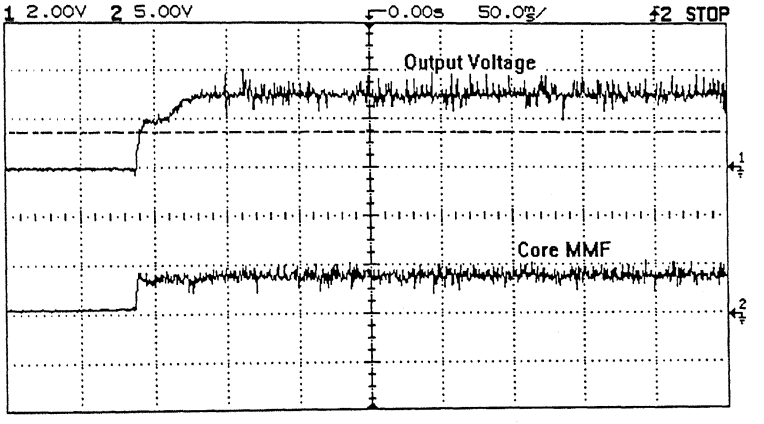


Fig. 5.13 Oscillogram of core mmf and output voltage for output voltage of 15V and input voltage of 20V at a load of 10 Ω.

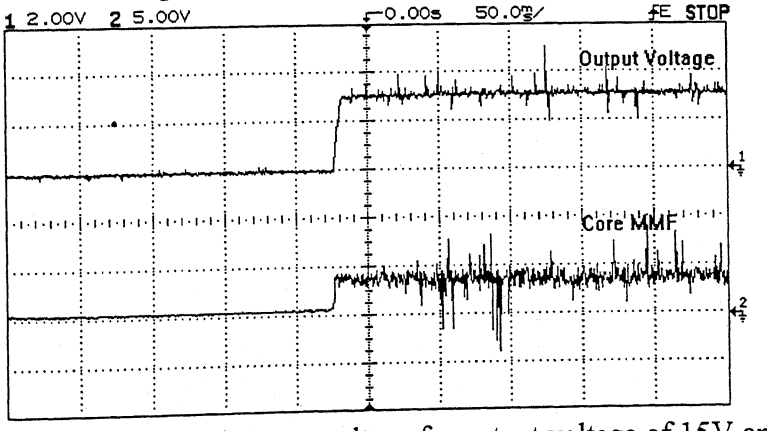


Fig. 5.14 Oscillogram of core mmf and output voltage for output voltage of 15V and input voltage of 30V at a load of 150 Ω.

The effect of load change has been experimented and the results for resistance changing from $R = 150\Omega$ to $R = 10\Omega$ is shown in Fig. 5.16, whereas the result for change in resistance from $R = 10\Omega$ to $R = 150\Omega$ is given in Fig. 5.17. Again it can be seen from these figures that they match closely with the simulation results in the sense that the average voltage remains unchanged.

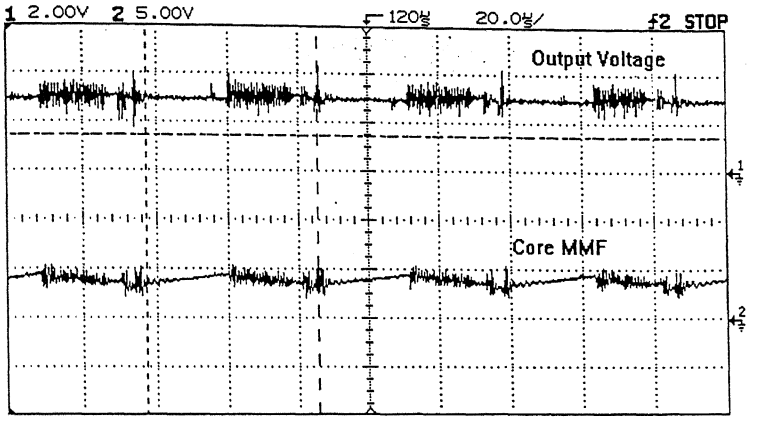


Fig. 5.15 Oscillogram of details core mmf and output voltage of Fig. 5.13

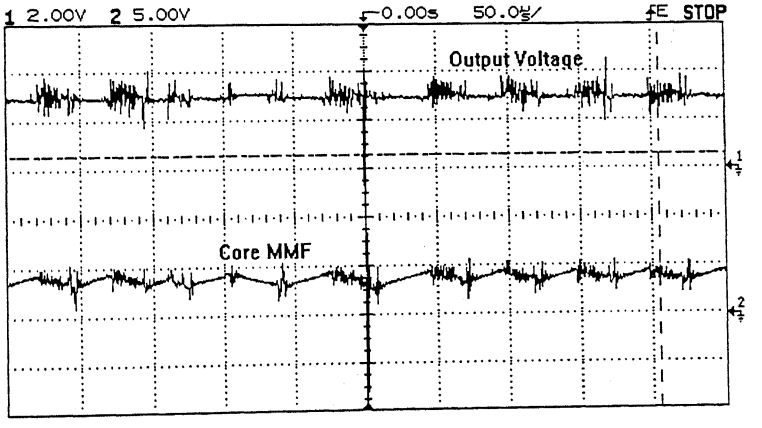


Fig. 5.16 Load changed from 150 Ω to 10 Ω when the input voltage is 20V.

The experiment for supply disturbance has not been carried out. The core mmf and leakage inductance has also made the waveform noisier than the simulated waveform.

5.3.2 Experimental Results for Boost Mode

The experimental results of the converter in its boost mode of operation is summarized in Table 5.4.For all the experiments in this mode, the input voltage V_{dc} has been taken to be 10 V and the output voltage V_0 is taken to be 15 V.

The converter has been set a reference output voltage of 15 V for a input voltage of 10V to show the boosting mode operation of the converter with the closed loop. The steady state waveforms along with the cold start behaviors are shown in Fig. 5.18 and 5.19. The detail steady sate waveforms for these conditions are shown in Fig. 5.20 and 5.21. The nature of cold start and steady state waveform matches closely with the simulation results shown in section 5.2.2.

Table 5.4 Experimental results of converter in Boost Mode

R_L	ΔR_L	Result shown in	Comments
150	---	Fig. 5.18	Steady state with cold start
10	---	Fig. 5.19	Steady state with cold start
150	---	Fig. 5.20	Steady state
10	---	Fig. 5.21	Steady state
150	-130	Fig. 5.22	effect of unload
20	130	Fig. 5.23	effect of load
150	-140	Fig. 5.24	Folding due to loading
10	140	Fig. 5.25	effect of unload

The closed loop characteristics in presence of load disturbance have been obtained. The results are given in Fig. 5.22 to Fig. 5.25. A step change of 130 Ω in load resistance does not change the average output voltage as can be seen from Fig. 5.22 and 5.23. However, when the change is 140 Ω as for the results shown in Fig. 5.24 and 5.25, the folding of the output voltage starts taking place.

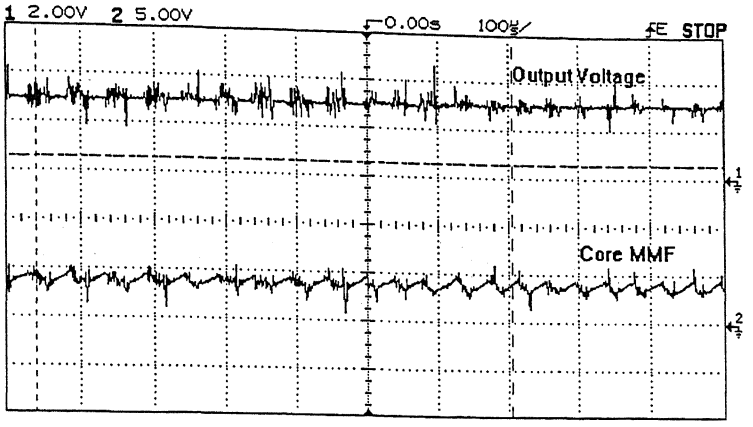


Fig. 5.17 Load changed from 10 Ω to 150 Ω when the input voltage is 20V.

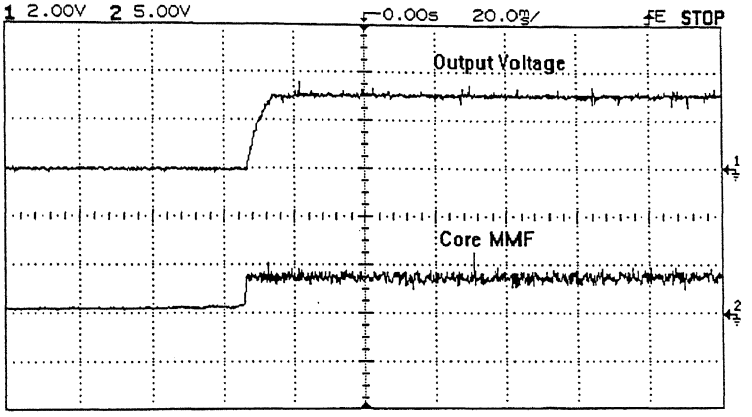


Fig. 5.18 Oscillogram of core mmf and output voltage for output voltage of 14V and input voltage of 10V at a load of 150 Ω.

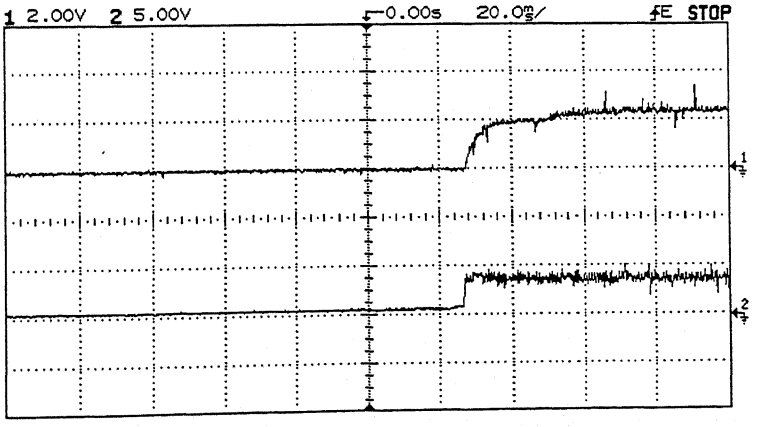


Fig. 5.19 Oscillogram of core mmf and output voltage for output voltage of 14 V and input voltage of 10V at a load of 10 Ω.

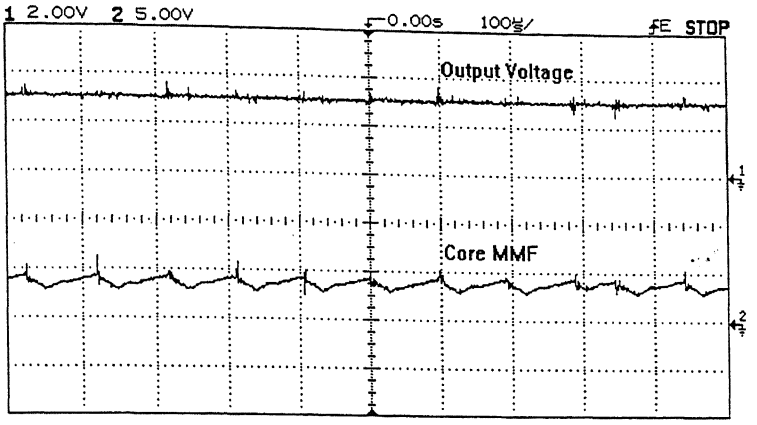


Fig. 5.20 Oscillogram of details core mmf and output voltage of Fig. 5.18

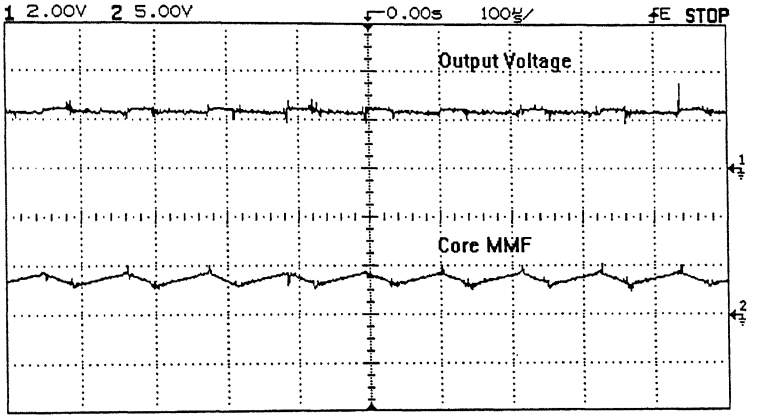


Fig. 5.21 Oscillogram of details core mmf and output voltage of Fig. 5.19

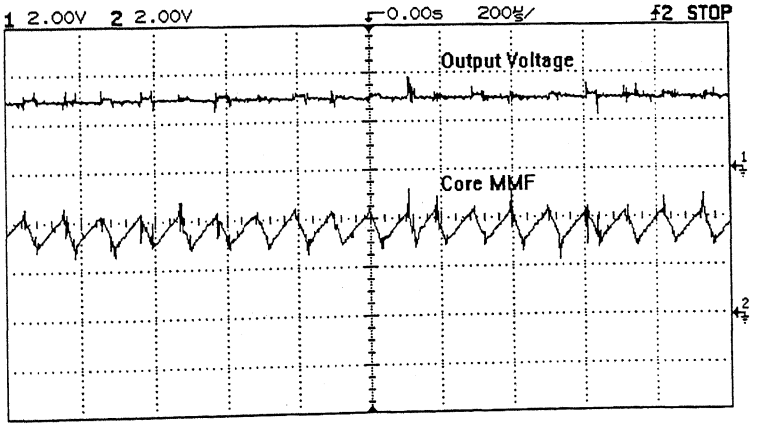


Fig. 5.22 Load changed from 150 Ω to 20 Ω when the input and output voltages are 10V and 14 V respectively.

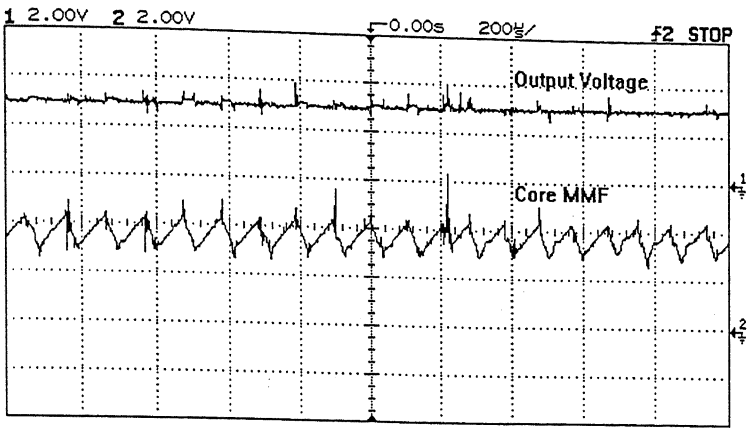


Fig. 5.23 Load changed from 20 Ω to 150 Ω when the input and output voltages are 10V and 14 V respectively.

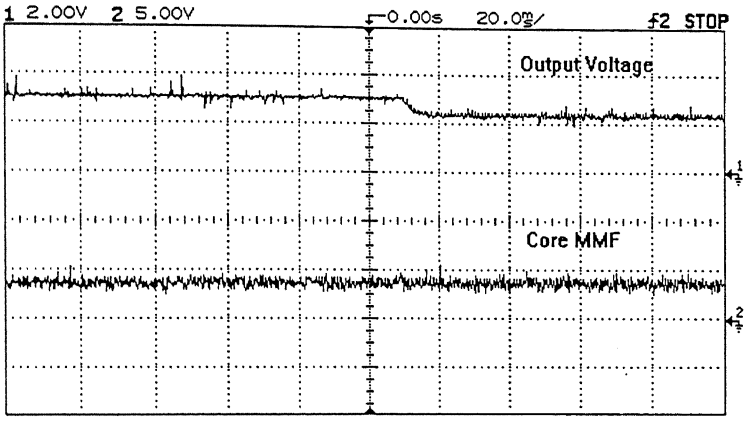


Fig. 5.24 Load changed from 150 Ω to 10 Ω when the input and output voltages are 10V and 14 V respectively. Folding characteristics starts appearing.

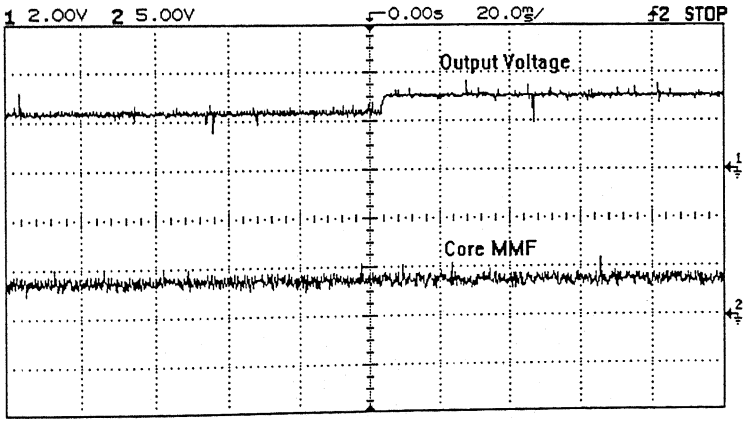


Fig. 5.25 Load changed from 10 Ω to 150 Ω when the input and output voltages are 10V and 14 V respectively.

5.4 HYSTERESIS CONTROL OF MULTIPLE (TWO) OUTPUT MODIFIED BUCK-BOOST CONVERTER

The two-output extension of the single output modified Buck-Boost converter is shown in Fig. 4.16. This converter has three switches and a diode. Due to large number of switches, it is obvious that small signal model of this converter will be much more complicated than others like multiple output conventional flyback converter with one switch or the single output modified converter. It therefore requires alternative method of closed loop control. In this section, a closed loop hysteresis controller has been proposed. This is an extension of the hysteresis control for the single output converter. The block diagram of the hysteresis controller for this converter is shown in Fig. 5.26. The performance of the closed lop controller has been tested by extensive simulation and experiments.

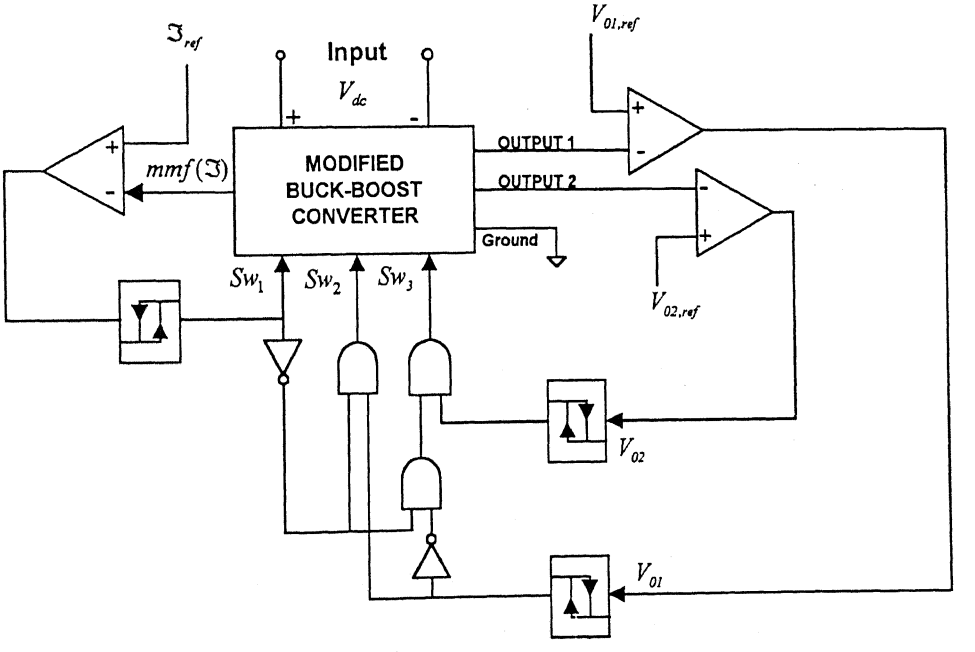


Fig. 5.26 Schematic diagram of hysteresis controller for two outputs modified Buck-Boost converter.

The closed controller uses three feedback loops. The first feedback loop is for core mmf, second for output 1 and third for the output 2. The core mmf controller is given the

top priority followed by controller for the output 1 and the output 2 is assigned last in the priority. The choice of the priority among the voltage loops is not strict and can be changed if required by the logic circuit. In Fig. 5.26, the voltage loop for output 1 is given higher priority compared to output 2. The switching ON of the load switch 1 is done when the switching state of the main switch is in OFF condition and similarly the switching ON of the load switch 2 is carried out when the main switch and load switch is simultaneously OFF.

The core mmf charging begins with switching ON of main switch Sw_m. Let this interval be denoted by t_{onM}. During this interval load switches Sw_1 & Sw_2 are open. The equivalent circuit under this condition is shown in Fig. 4.18(a). The main switch Sw_m turns off when the core acquires the assigned maximum value of the core mmf. If the output 1 has hit the minimum of the reference voltage then the load switch Sw_1 turns on. The equivalent circuit is shown in Fig. 4.18(b). Similarly, when the output capacitor gets charged to its peak reference value Sw_1 turns OFF due to hysteresis action and it allows load switch Sw_2 of output 2 to get turned ON. The equivalent circuit for load switch Sw_2 conducting is given in Fig. 4.18(c). The core mmf if has not hit the minimum value of the reference mmf then energy recovery takes place. The equivalent circuit of the optional energy recovery interval, where all the switches are open is given in Fig. 4.18(d).

5.5 ANALYSIS OF HYSTERESIS CONTROLLED CLOSED LOOP SYSTEM

The reference voltages for different outputs are set equal to the desired outputs and the ripple requirements decide the hysteresis bandwidth. It is necessary to get a criteria to choose a reference value of core MMF for given outputs and possible variations. It is assumed here that the ripple content of the core MMF and output voltages are very small. Let the core mmf is operated with hysteresis band of $\Delta\Im$ around an average core mmf of $\Im_{av}$ and let the ON for a period of main switch, load switch 1 and load switch 2 be denoted by t_{onM}, t_{on1} and t_{on2} respectively. These intervals can be calculated from the averaging technique and are given by,

$$t_{onM} = \frac{\Delta\Im}{N_1 V_{dc}} L_1 \qquad \& \qquad t_{on1} \approx \frac{\Delta\Im}{N_1 V_{o1}} L_1 \qquad t_{on2} \approx \frac{\Delta\Im}{N_1 V_{o2}} L_1 \tag{5.8}$$

The average core MMF calculated over any subinterval in a cycle must be equal to the average value over a cycle since the ripple in the MMF is small. Thus,

$$F_{av} = N_1 \left(\frac{T}{t_{on1}}\right)\left(\frac{V_{01}}{R}\right) \tag{5.9}$$

where $T = t_{onM} + t_{on1} + t_{on2}$ is the cycle period if there is no energy recovery. Solving (5.8) and (5.9) we obtain (5.10).

$$F_{av} = \left(\frac{N_1 V_{01}}{R_1}\right)\left(1 + \frac{V_{01}}{V_{dc}} + \frac{V_{01}}{V_{02}}\right) \tag{5.10}$$

In order to calculate the reference MMF for this experiment, we calculate the MMF from (5.10) and perform the simulation study starting with this value. The actual reference MMF is 50% to 60% of the calculated average MMF as calculated from (5.10). The critical resistance for outputs can be calculated in the same line as done for the single output.

5.6 SIMULATION RESULTS OF TWO OUTPUT CONVERTER

There are four possible modes of operation of the multiple output modified Buck-Boost converters. These are as follows.

- Both Outputs are operating in Buck mode
- Both outputs are working in Boost mode
- Output 1 is in Buck mode and Output 2 in Boost mode
- Output 1 in Boost mode and Output 2 in Buck mode

The simulation study has been carried out for all the four cases. The results and discussion will be presented next.

The summary of the simulation study for converter operation in Buck mode with possible disturbances is given in Table 5.5. The output voltages of the output 1 and output 2 are 12 V and 6 V respectively. The nominal load resistances are 25 Ω and 15 Ω for output 1 and output 2 respectively. Simulation study has been carried out for cold start behavior, load and source disturbances when acting alone and when they are acting together. The disturbance in supply or load (if any) has been marked by an arrow in the simulation results presented below.

With the nominal resistance connected to both the outputs, simulation has been carried to observe the cold start behavior. The result is shown in Fig. 5.27. The core MMF builds up first to the maximum of the reference MMF and then it charges first the output 1. The charging of the capacitor of the output 1 takes few cycles. During this interval the output 2 remains in zero state. Once the output 1 reaches the reference voltage, the charging of the output 2 begins. The two outputs can be simultaneously charged if the special magnetic circuit arrangement are made as given in [54]. It is to be noted that the reference core MMF is taken to be less than 50 % of the MMF calculated from (5.10). Due to this the ripple magnitude is slightly higher than the specified. This can be easily seen from the waveforms at lighter loads when the output voltage obeys the ripple limits.

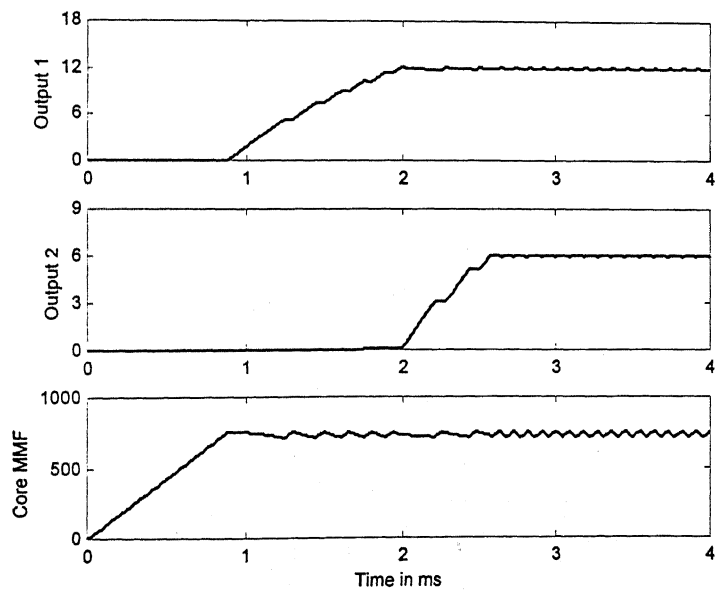


Fig. 5.27 Cold start behavior of the converter

Table 5.5 Simulation Results of the converter in Buck mode

V_{dc}	ΔV_{dc}	R_1	ΔR_1	R_2	ΔR_2	$V_{o1,ref}$	$V_{02,ref}$	Result Shown in	Comments
20	---	25	---	15	---	12	6	Fig. 5.27	Cold Start Behavior
20	10	25	---	15	---	12	6	Fig. 5.28	Supply Disturbance
20	-5	25	--	15	--	12	6	Fig. 5.29	Supply Disturbance
20	--	25	25	15	--	12	6	Fig. 5.30	Load Disturbance on Output 1
20	--	25	-10	15	---	12	6	Fig. 5.31	Load Disturbance on Output 1
20	---	25	---	15	25	12	6	Fig. 5.32	Load Disturbance on Output 2
20	---	25	---	15	-10	12	6	Fig. 5.33	Load Disturbance on Output 2
20	--	25	25	15	25	12	6	Fig. 5.34	Load Disturbance on Output 1 & 2
20	--	25	-10	15	-10	12	6	Fig. 5.35	Load Disturbance on Output 1 & 2
20	--	25	-10	15	25	12	6	Fig. 5.36	Load Disturbance on Output 1 & 2
20	--	25	25	15	-10	12	6	Fig. 5.37	Load Disturbance on Output 1 & 2
20	-10	25	-10	15	-10	12	6	Fig. 5.38	Load & supply Disturbance on Output 1 & 2
20	10	25	25	15	25	12	6	Fig. 5.39	Load & supply Disturbance on Output 1 & 2

The supply disturbance changes the frequency of the MMF waveform and hence the turn ON and OFF periods of the switches in the circuit. However, the duty ratio remains the same. There is a slight change in the ripple magnitude also due to changed frequency of the core MMF. The effect of the positive supply disturbance is shown in Fig. 5.28 whereas Fig. 5.29 shows the effect of negative supply disturbance.

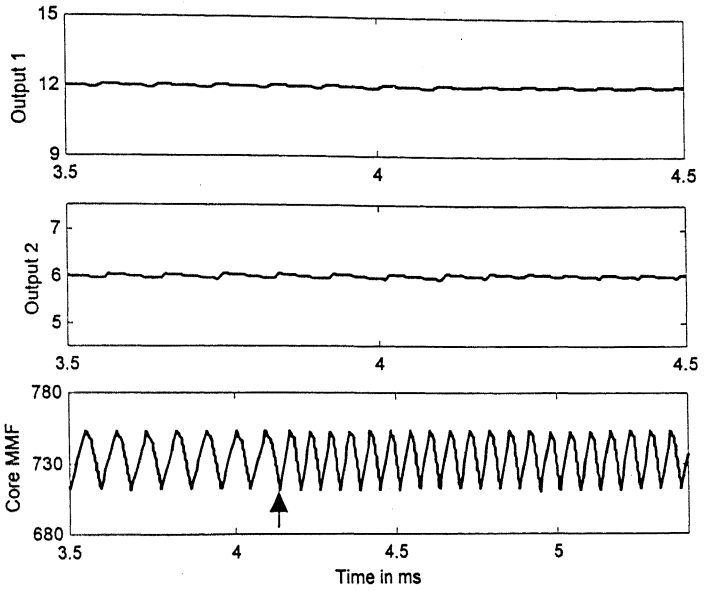


Fig. 5.28 Effect of supply disturbance, supply going up by 10V

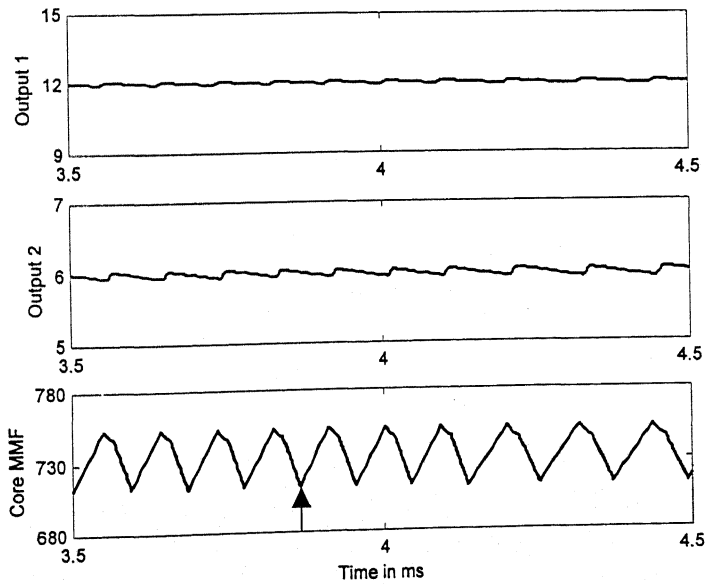


Fig. 5.29 Effect of supply disturbance, supply lowered by 5V.

The simulation results for load disturbance on one the outputs are given in Fig. 5.30 to 5.33. This is to show the regulation and cross-regulation due to load disturbances. Simulation studies on simultaneous load disturbances are given in Fig. 5.34 to 5.37. It can be seen from these figures that the cross regulation is almost zero. The effect of the load change results in change in the ripple magnitude of the output, if the load change is within the permissible limits. The core MMF adjusts its energy recovery interval in order to regulate the output voltages. The effect of excess loading can be seen from Fig. 5.33. The output voltage shows not only increase in the ripple magnitude but also the average output voltage also decreased. This shows the folding characteristics of output 2 whereas output 1 remains unaffected.

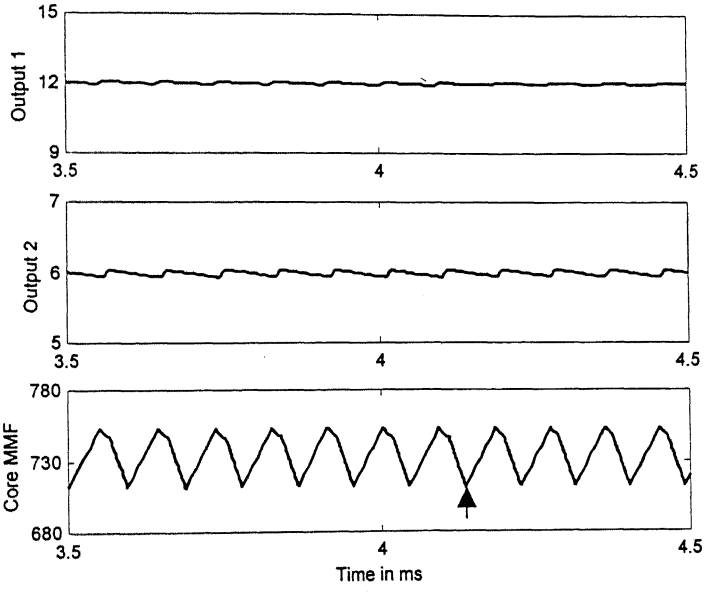


Fig. 5.30 Effect of Load disturbance on Output 1, resistance increased by 25Ω.

Similar effect can be seen in Fig. 5.35. The output 2 shows a dip in the output voltage whereas the output 1 remains unaffected. Since the output 1 is given more priority, the output voltage of output 1 remains unchanged. In the extreme conditions, Output 2 may collapse totally whereas the output 1 continues to regulate. This configuration is therefore better than the others, where there is strong correlation between the outputs and any change in supply or the load affects all the outputs.

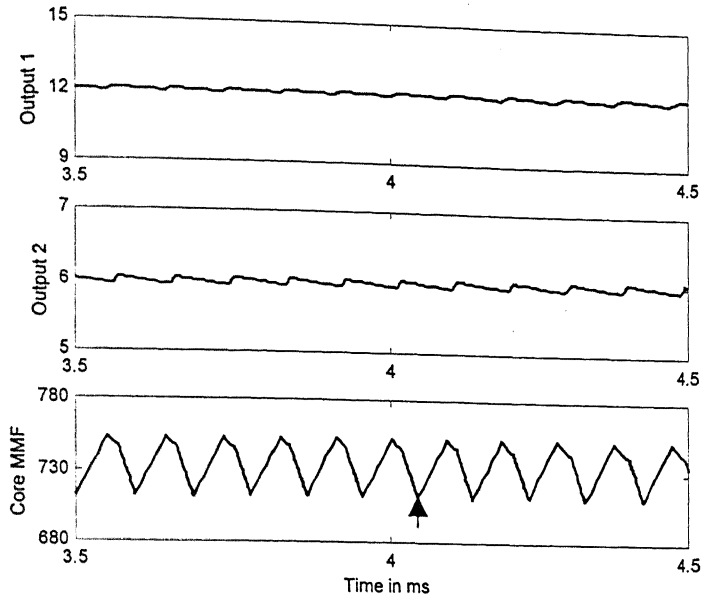


Fig. 5.31 Effect of Load disturbance on Output 1, resistance decreased by 10Ω.

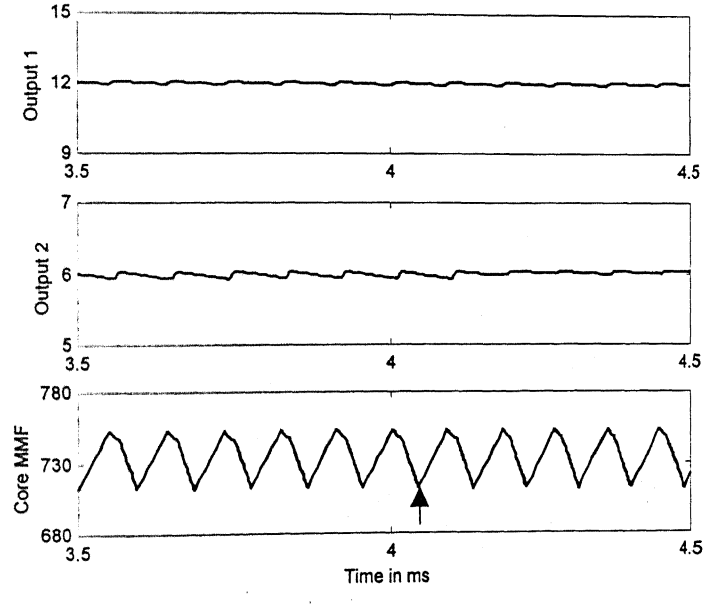


Fig. 5.32 Effect of Load disturbance on Output 2, resistance increased by 25Ω.

It is possible to design the transformer windings of the isolated multiple output Buck-Boost converters shown in Fig. 4.16 which will allow simultaneous charging of both the outputs. In such configuration both the outputs uses the core MMF for changing the outputs. Thus, if

the core MMF is not sufficient to cater the loads, then output voltages of all the outputs will be lower then the reference value. This can happen due to excess loading of any one the outputs or a large dip in the supply. If the regulation is due loading of one of the outputs, this is called cross-regulation. Thus, the sequential charging of the output capacitors of proposed topology although require a higher MMF but the cross regulation is not a problem. But, assigning the priority among the outputs is normally difficult. We do not have loads where we can sacrifice one output and work with the other.

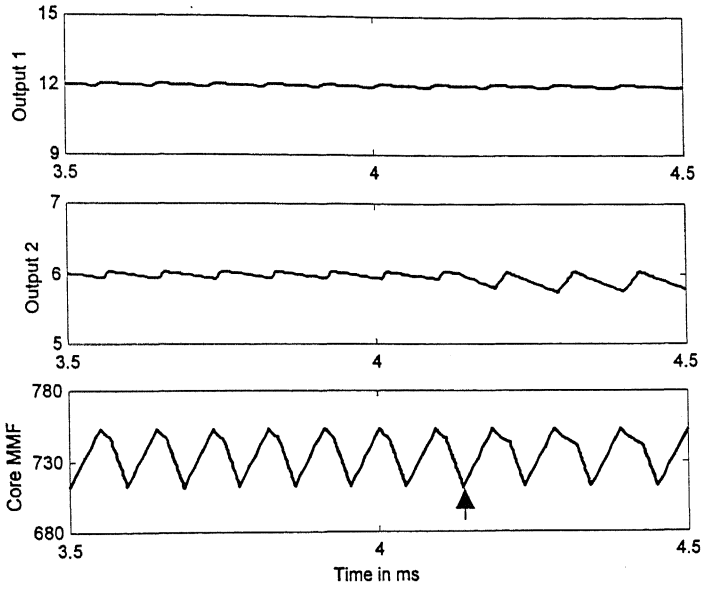


Fig. 5.33 Effect of Load disturbance on Output 2, resistance decreased by 10Ω.

Two extreme disturbances possible on any converter have been simulated for this closed loop converter system. The supply and load goes down simultaneously. The loads require more power and source starts delivering less power. The simulation result is shown in Fig. 5.38. Output 1 shows an increase in the ripple content but the average voltage remains same, whereas the output 2 has large ripple content and operates at lower average output voltage. In the other case both the output resistance and supply voltage has undergone a step increase, there is no change in any of the outputs. The frequency of the ripple of the core MMF goes up and the energy recovery duration shows contraction. If the loading is sufficiently increased, the folding characteristics starts appearing. The output 2 gets affected more compared to output1.

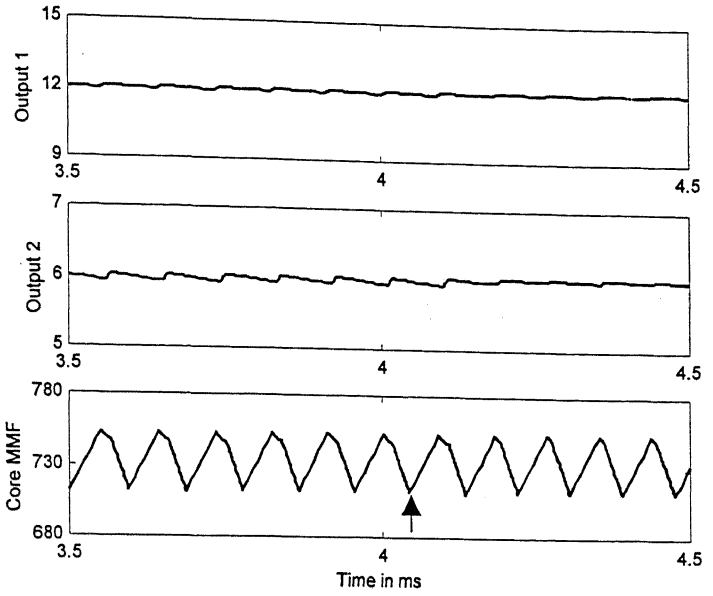


Fig. 5.34 Effect of Load disturbance on Output 1 & 2, both resistance increased by 25Ω.

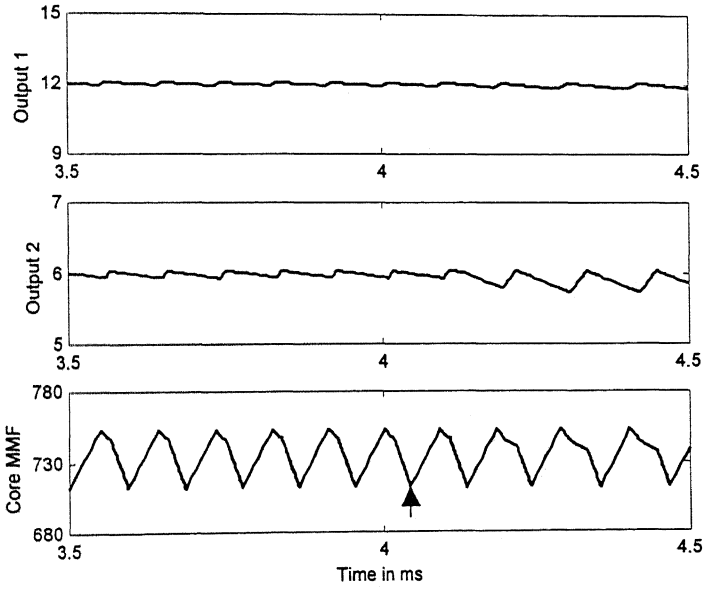


Fig. 5.35 Effect of Load disturbance on Output 1 & 2, both resistances decrease by 10 Ω.

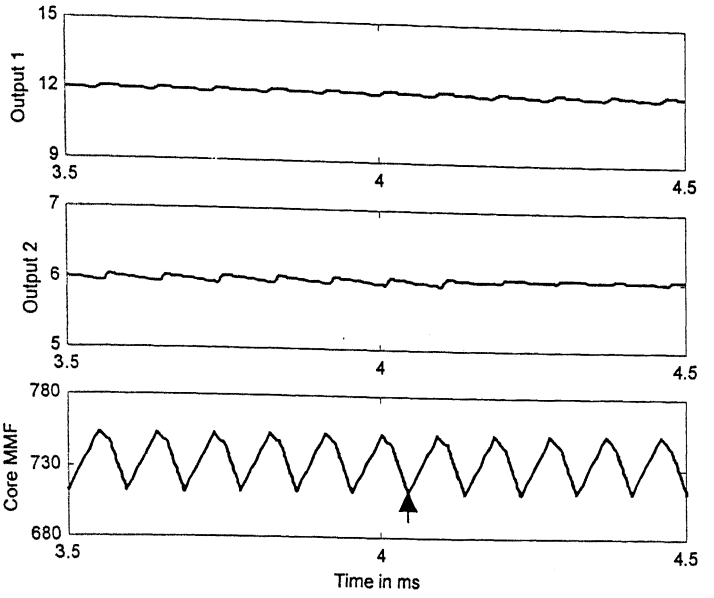


Fig. 5.36 Effect of Load disturbance on Output 1 & 2, resistance of output1 decreased by 10 Ω and resistance of output 2 increased by 25 Ω.

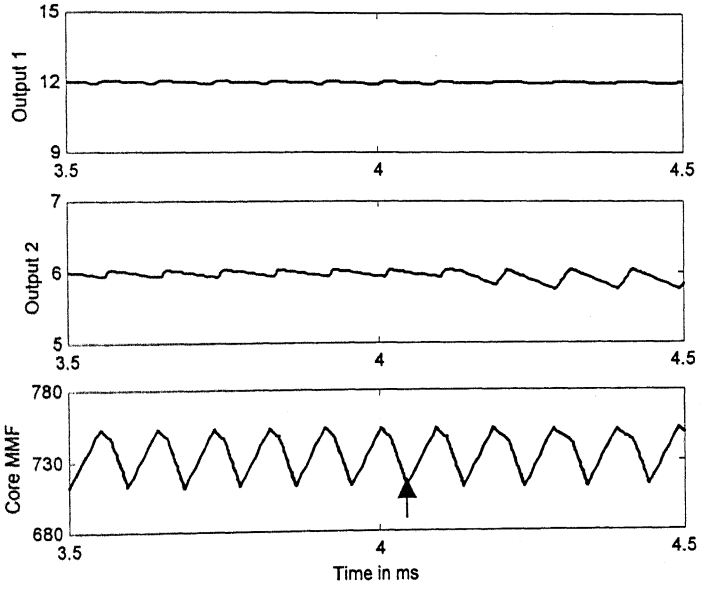


Fig. 5.37 Effect of Load disturbance on Output 1 & 2, resistance of output increased by 25 Ω and resistance of output 2 decreased by 10 Ω.

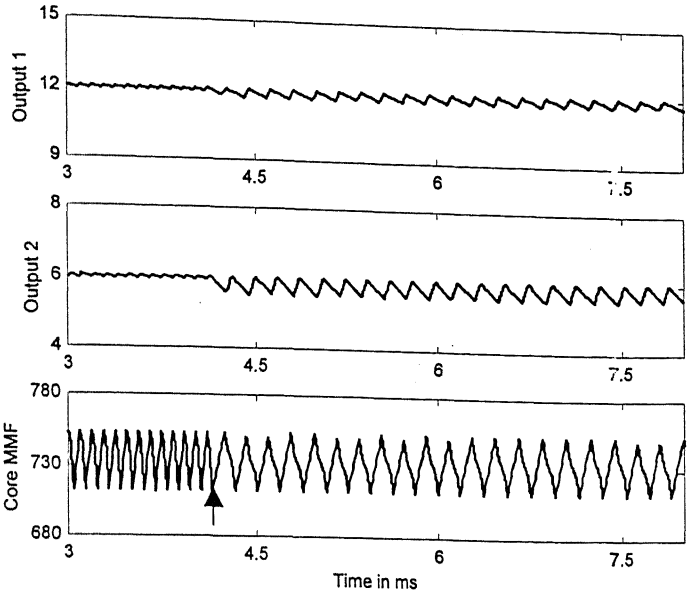


Fig. 5.38 Effect of combined Load and supply disturbance on Output 1 & 2, both resistance decreased by 10 Ω and supply dips by 10V.

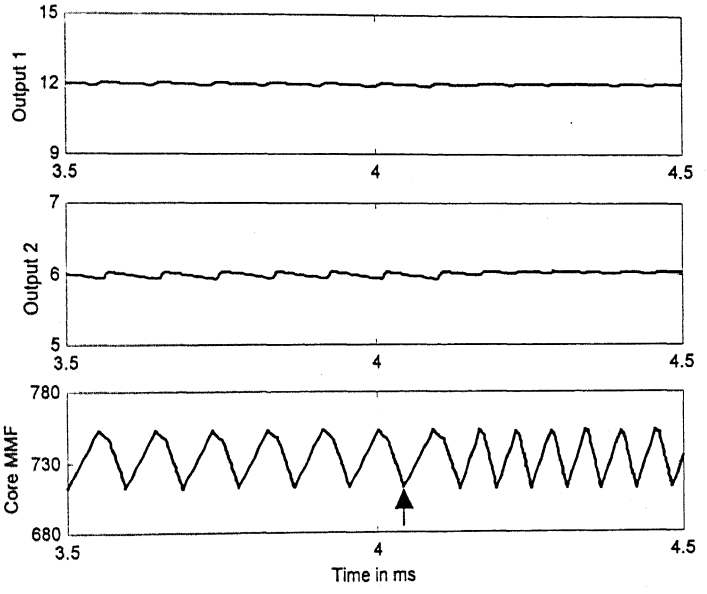


Fig. 5.39 Effect of combined Load and supply disturbance on Output 1 & 2; both the Output resistances increased by 25 Ω and supply rises by 10V.

The summary of the simulation result for the close loop operation in other possible modes of converter operation is given in Table 5.6. Th converter operation with one output buck and another in boost mode is given in Fig. 5.40 and 5.41. The behavior of the cold start is similar to buck mode operation presented in Fig. 5.27. The parameters of the

converter are taken to be same as for buck mode. The ripple contents in the outputs are function of the loading and core MMF. It can be seen from Fig. 5.42 that the cold start behavior with both outputs in Boost mode is similar to rest. The disturbance performance has been studied extensively and results are similar as to that of the buck mode operation of the converter.

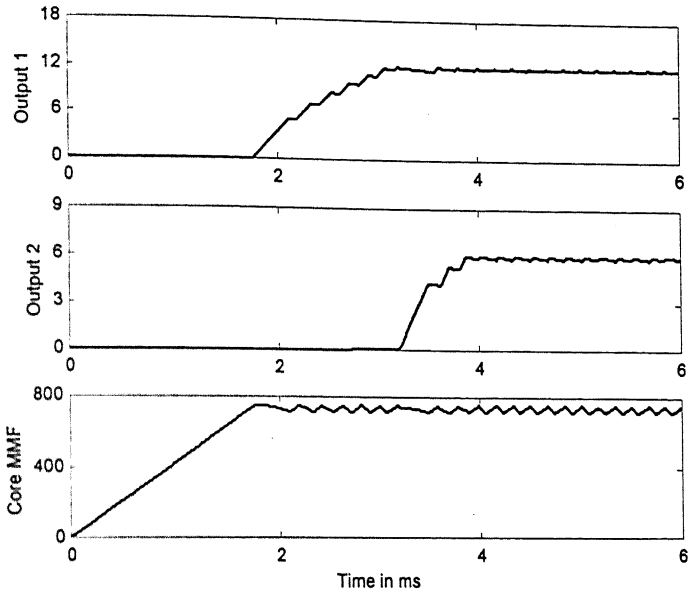


Fig. 5.40 Cold start behavior for converter with Outputs 1 & 2 in Buck & Boost Modes respectively

Table 5.6 Simulation Results of the converter in Buck mode

V_{dc}	ΔV_{dc}	R_1	ΔR_1	R_2	ΔR_2	V_{o1}	V_{02}	Result Shown in	Comments
10	---	25	---	15	---	12	6	Fig. 5.40	Output 1 in Buck & Output 2 in Boost Mode
10	---	15	---	25	---	6	12	Fig. 5.41	Output 1 in Boost & Output 2 in Buck Mode
10	---	15	--	15	--	12	15	Fig. 5.42	Both Outputs in Boost Mode

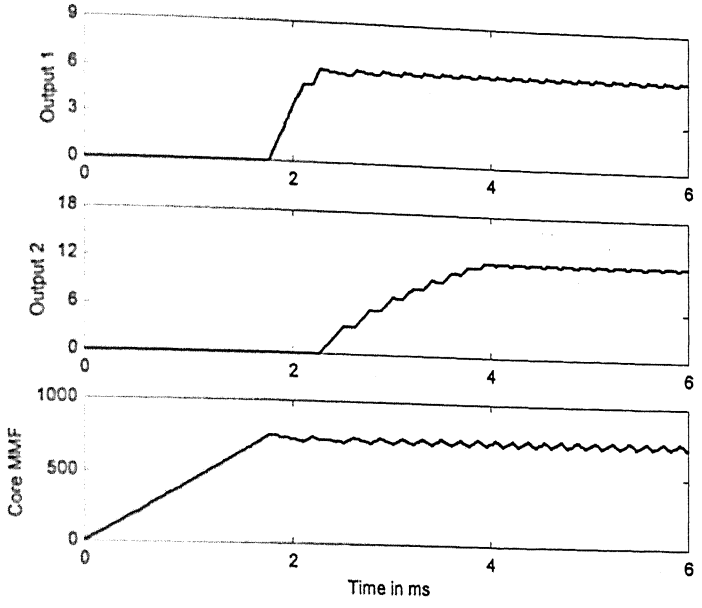


Fig. 5.41 Cold start behavior for converter with Outputs 1 & 2 in Boost & Buck Modes respectively

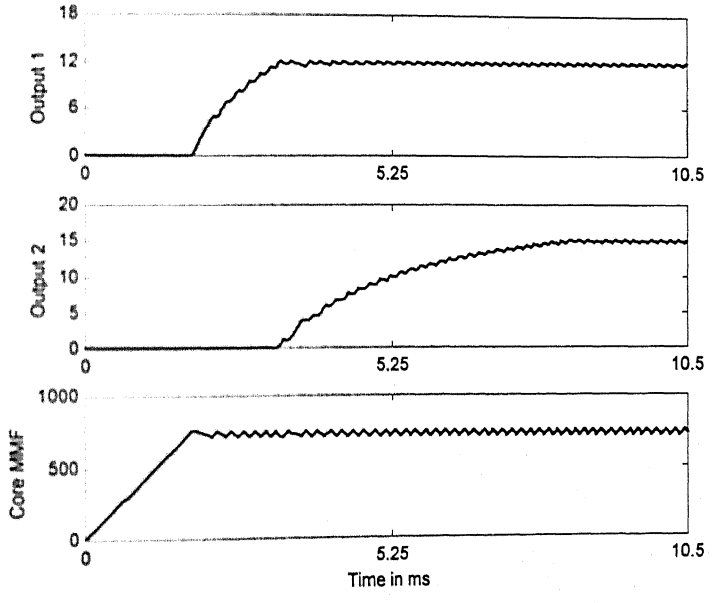


Fig. 5.42 Cold start behavior for converter with both Outputs 1 & 2 in Boost Mode

5.7 EXPERIMENTAL RESULTS

The experiment has been carried out to verify the some of the simulation results. The details of hardware fabrication and their parameters are given in Chapter 6. The

summary of the experimental results presented in this section is given in Table 5.7. The scaling factors for voltages at output 1 and 2 are respectively 4.82 and 2.85 in the oscillograms i.e. waveforms of the variables shown on the oscilloscope. The core MMF has got a scaling factor of 150. The experiments are carried out at low frequency as the energy recovery transformer has got a considerable leakage inductance and hence coupling noise among the windings are high. The frequency of operation can be made high if a better energy recovery winding is used.

Table 5.7 Experimental Results for Multiple (Two-) Output Buck-Boost Converter

V_{dc}	R_1	ΔR_1	R_2	ΔR_2	V_{01}	V_{02}	Shown in Fig. No.	Comments
10	50	---	40	---	15	5	Fig. 5.43	Output 1 in Boost & Output 1 in Buck Mode
10	50	---	40	---	15	5	Fig. 5.44	Steady state waveforms
10	50	---	40	---	15	5	Fig. 5.45	Steady state waveforms
10	50	---	40	---	15	5	Fig. 5.46	Cold start Behavior
10	50	---	40	---	15	5	Fig. 5.47	Cold start Behavior
10	50	---	40	---	15	5	Fig. 5.48	Cold start Behavior
10	50	100	40	---	15	5	Fig. 5.49	Load Rejection on Output 1
10	150	-100	40	---	15	5	Fig. 5.50	Effect of Loading
10	50	---	40	100	15	5	Fig. 5.51	Load Rejection on Output 2
10	50	---	140	-100	15	5	Fig. 5.52	Effect of Loading

Fig. 5.43 to Fig. 5.45 shows the steady state behavior of the closed loop converter operation. The two outputs in steady state is shown in Fig. 5.43, whereas the oscillograms shown in Fig. 5.44 and 5.45 is for outputs 1 and 2 with respect to the core MMF waveforms. The ripple contents in the output voltages are within the specified limits. The core MMF has got a hysteresis bandwidth of 50 % of the maximum value. If this limit is made smaller the ripple frequency will go up. All the output shows a number of high

amplitude short-lived spikes. These quantities on magnification are found to oscillations of the order of MHz. These oscillations are due switching and transformer coupling.

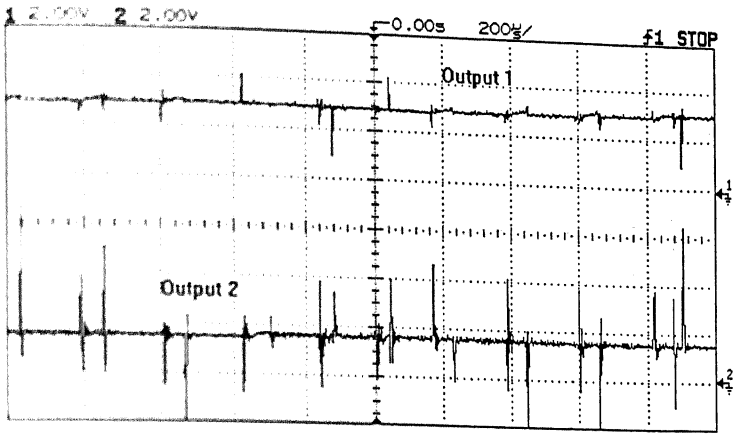


Fig. 5.43 Output voltages in steady state both outputs

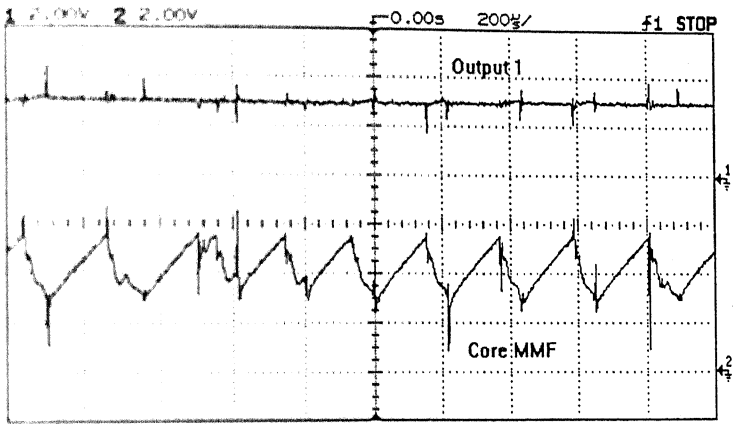


Fig. 5.44 Experimental waveforms of Output voltage 1 and core MMF in steady state

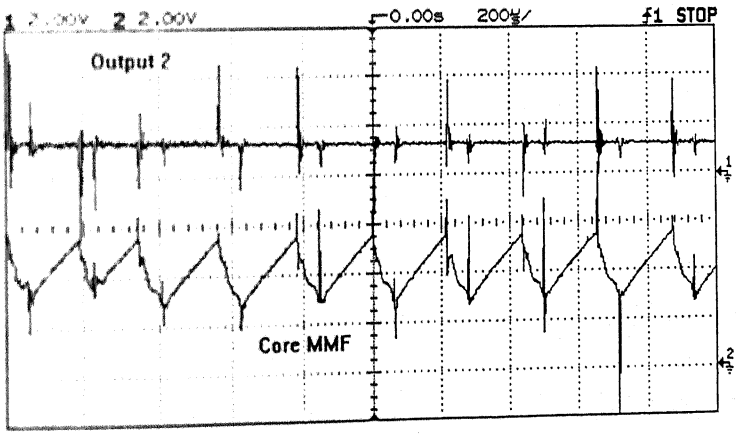


Fig. 5.45 Experimental waveforms of Output voltage 2 and core MMF in steady state

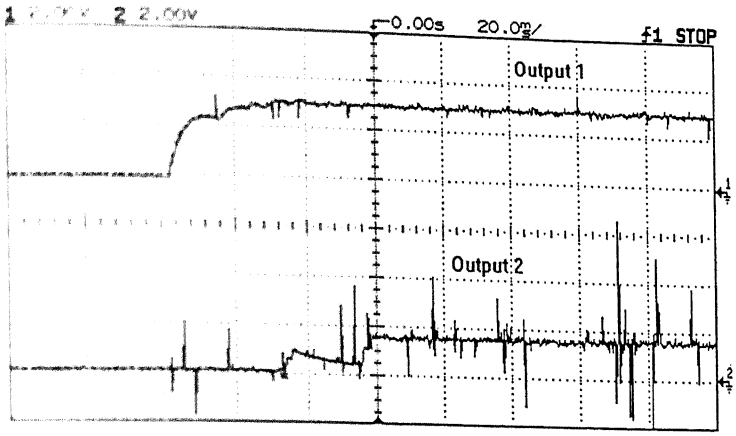


Fig. 5.46 Experimental waveforms of Outputs 1 & 2 for cold start.

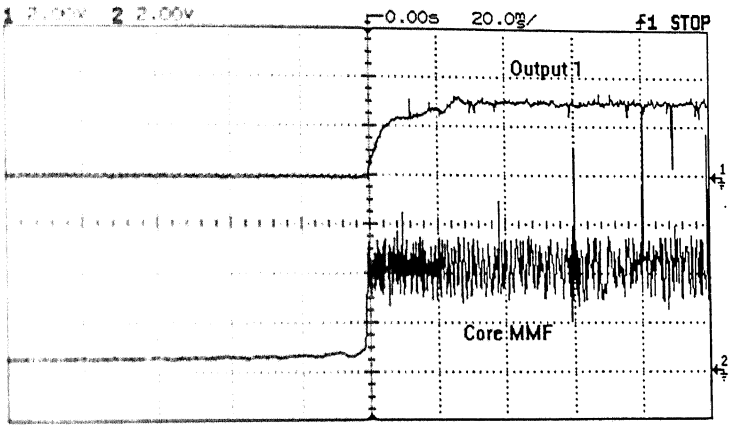


Fig. 5.47 Experimental waveforms of Outputs 1 and core MMF for cold start.

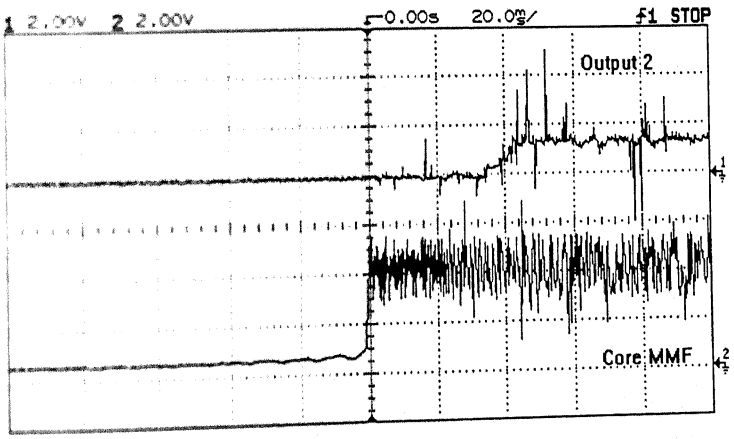


Fig. 5.48 Experimental waveforms of Outputs 2 and core MMF for cold start.

The cold start characteristics of the converter with hysteresis controller have been verified in experiment. The results are given in Fig. 5.46,5.47 and 5.48. It can be seen from Fig. 5.47 that the charging of output 2 begins after output 1 has reached its reference value.

here is a small dip in the output voltage due to some unknown disturbance for a small duration. But the output 2 is able to restore the reference voltage.

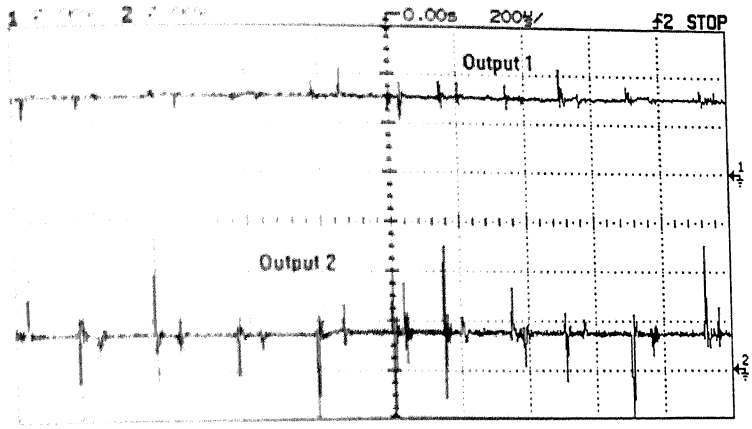


Fig. 5.49 Experimental waveforms of Outputs 1 & 2 when load is rejected on output 1.

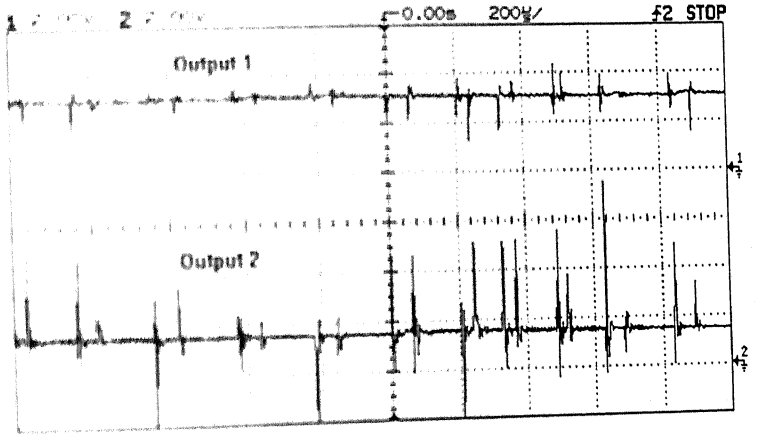


Fig. 5.50 Experimental waveforms of Outputs 1 & 2 when load on output 1 is increased.

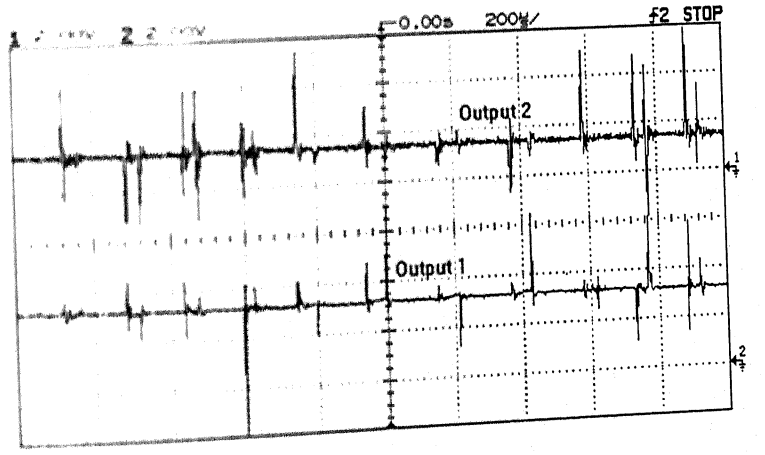


Fig. 5.51 Experimental waveforms of Outputs 1 & 2 when load is rejected on output 2.

The effect of load disturbances has been carried out in laboratory. The results of these experiments are presented here in Fig. 5.49 to 5.52. It can be seen from these oscillograms that the effect of load disturbance does not affect either of the outputs.

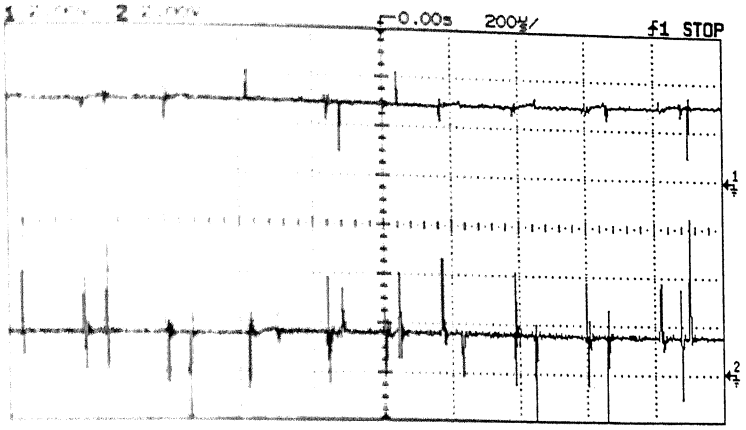


Fig. 5.52 Experimental waveforms of Outputs 1 & 2 when load on output 2 is increased.

5.8 CONCLUSION

A closed loop control strategy for modified Buck-Boost converter has been presented in this chapter. The proposed controller for the modified converter is capable of regulating the disturbances in the same cycle. The output remains unaffected in presence of the acceptable limits of disturbances in source and load. The closed loop hysteresis controller is also capable of compensating the disturbances in the multiple output converter topology. The closed loop converter system has been verified by extensive simulation and some experiments.

In conclusion, the modified Buck-Boost converter with hysteresis controller has faster dynamic response for load change, supply disturbance. The closed loop converter can track larger change in the output voltage as compared to conventional Buck-Boost converter. However, the modified converter requires a coupled inductor, an additional switch and a diode.

$R_1 = R_2 = 39K, R_3 = 18K, R_4 = 100K, R_5 = R_6 = 6.8K R_7 = 2.7K, R_8 = R_9 = 33\Omega,$
$R_{10} = 2K, R_{11} = R_{12} = 3.9K R_{13} = 12K, R_{14} = 10K, P_1 = 100K, P_2 = 22K$
$C = 100pF$

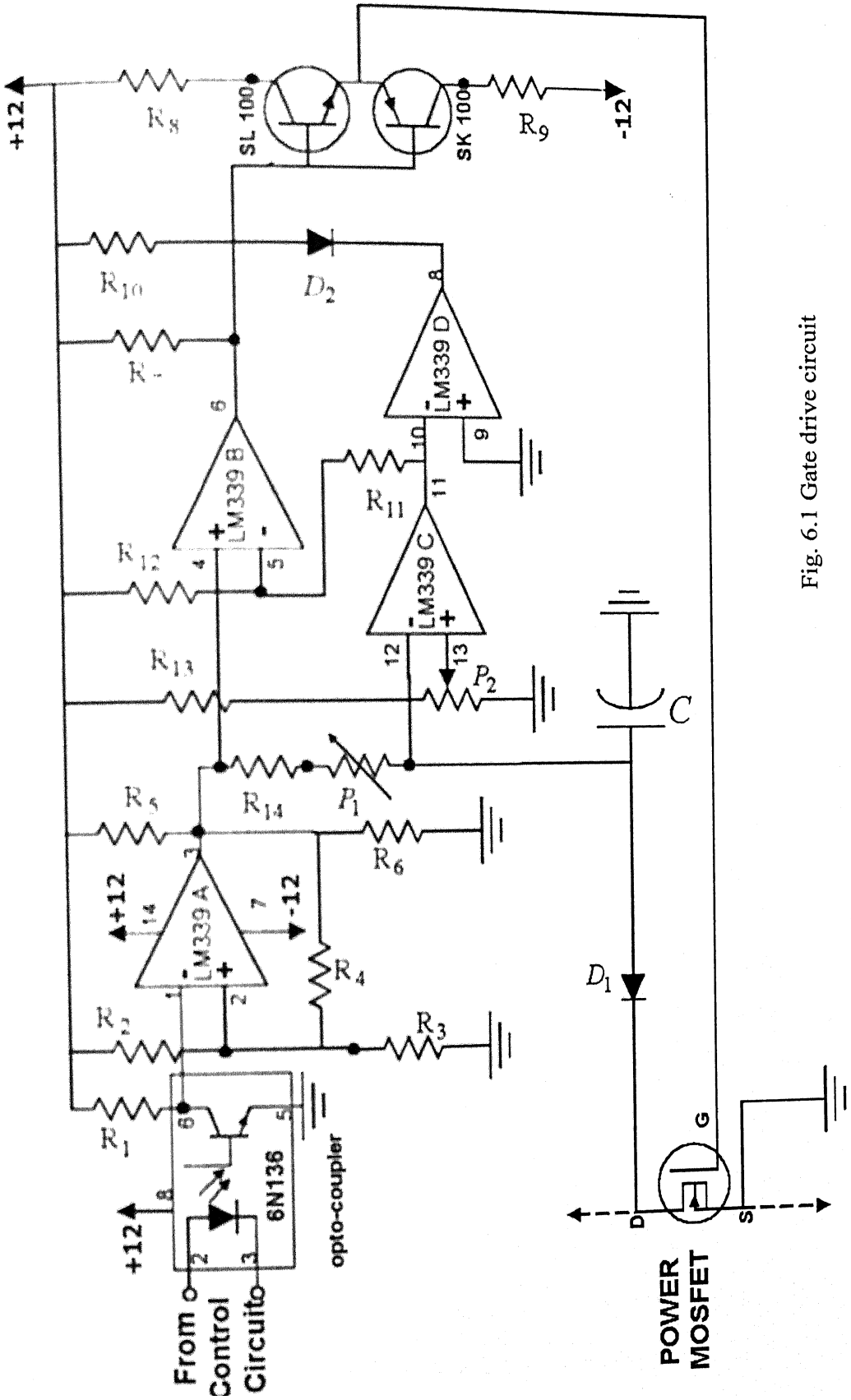


Fig. 6.1 Gate drive circuit

The drain-source voltage across MOSFET increases with drain current at a given gate to source voltage. This forms the basis for over current protection of the power device. The potentiometer P2 shown in Fig. 6.1 is set such that the voltage at variable point is one diode drop more than the drain source voltage corresponding to the peak value of the normal drain current. A RC circuit delays activation of protection circuit to avoid malfunctioning of the switch in case the power circuit has transient over current. If the drain current is within the normal limit, the drive signal from the control circuit is transmitted to the gate of the power MOSFET. However, if the drain current exceeds its limiting value and sustains for more than a pre-specified period, the protection logic operates and stops the control signal from reaching the gate. The drive circuit issues OFF signal for the power device and LED D_2 glows indicating fault. The fault indication persists as long as the turn-on process is present. An isolated power supply has been used for the drive circuit for the isolation of the gate from the control circuit. The circuit diagram of the isolated power supply for driver circuit is shown in Fig. 6.2. Transformer at ac mains in the power supply for the driver circuit provides the electrical isolation. It is to be noted that the power supply is a linear power supply. Since the power rating of the driver circuit is less and hence this has been used rather than a switched mode power supply. The component values for this power supply is shown in the figure.

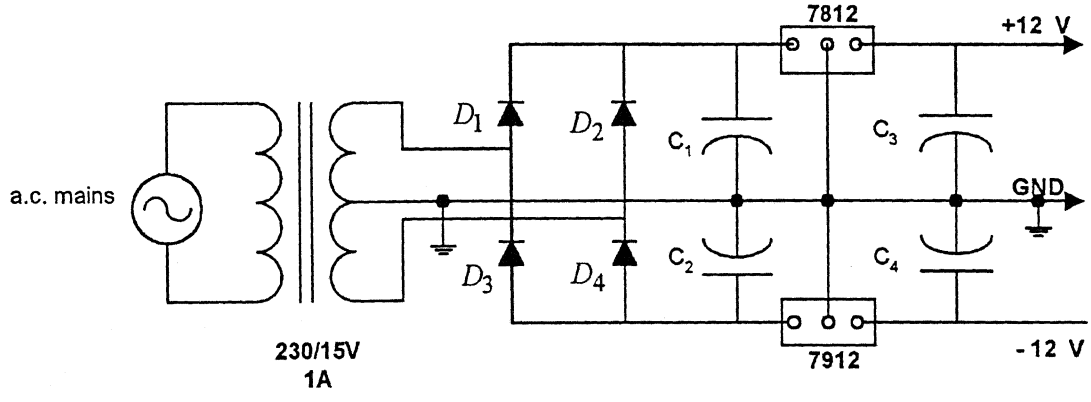


Fig. 6.2 Isolated power supply for gate driver circuit

The drive circuit has a delay of nearly $1\mu Seconds$ between the applied input and the output of the drive circuit. The largest delay is observed in the Opto-Isolator unit. Therefore a high speed Opto-Isolator can be used in place of 6N136 used in this

circuit to reduce the overall delay of the drive circuit. With the present circuit, the drive circuit can work successfully up to 200 kHz. At a higher frequency than this, the output is not only significantly delayed but also starts showing distortions in the output.

6.2 BUCK-BOOST CONVERTER

In a conventional Buck-Boost converter circuit, we have a power MOSFET switch, a fast recovery diode and a capacitor. The load of DC-DC converter can be approximated by time varying resistance. In the experiments, the load is realized by a static resistance. The block diagram representation of the complete system is shown in Fig. 6.4. The power supply for all the units are isolated and represented in figure by different grounding symbol. Due to isolated power supplies used for each of the blocks of the circuit, all the units are electrically isolated from each other. The isolation provides electrical protection of each unit from the other and simultaneously it restricts cross signal interference.

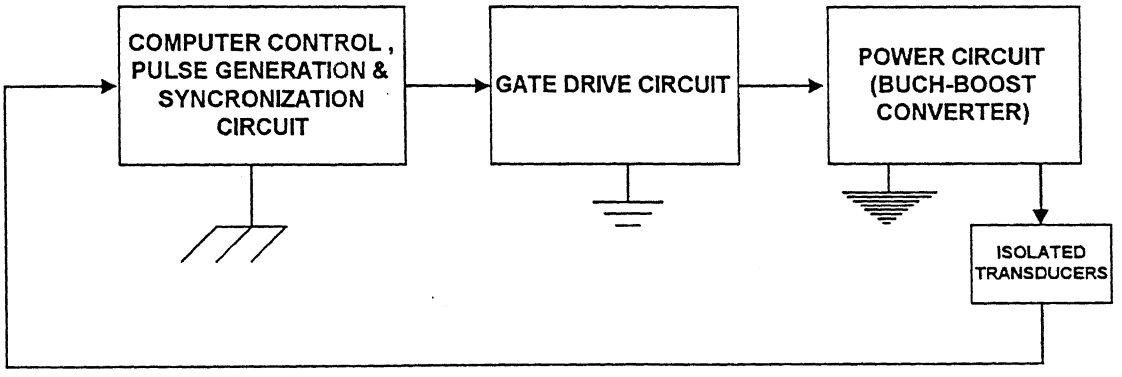


Fig. 6.3 Block diagram of overall system

The circuit diagram power circuit of the Buck-Boost converter is given in Fig. 6.4. This circuit also includes transducers used for the measurement of the states of the converter.

The power circuit of converter is designed for following parameters:

$$L = 3mH, r_L = 1.2\Omega, C = 330\mu F, esr = 20m\Omega, R = nominal\ load\ resistance = 64.02\Omega$$

$$V_{dc} = 10V\ to\ 20V, \quad f = 26\,kHz, \quad rated\ maximum\ inductor\ current = 4A$$

The symbols for the converter specification have usual meaning. The input voltage of the converter is expected to be 10 V or 20 V. The converter is designed to operate at 26 kHz. However, the circuit is tested to operate at 26 kHz and 54 kHz.

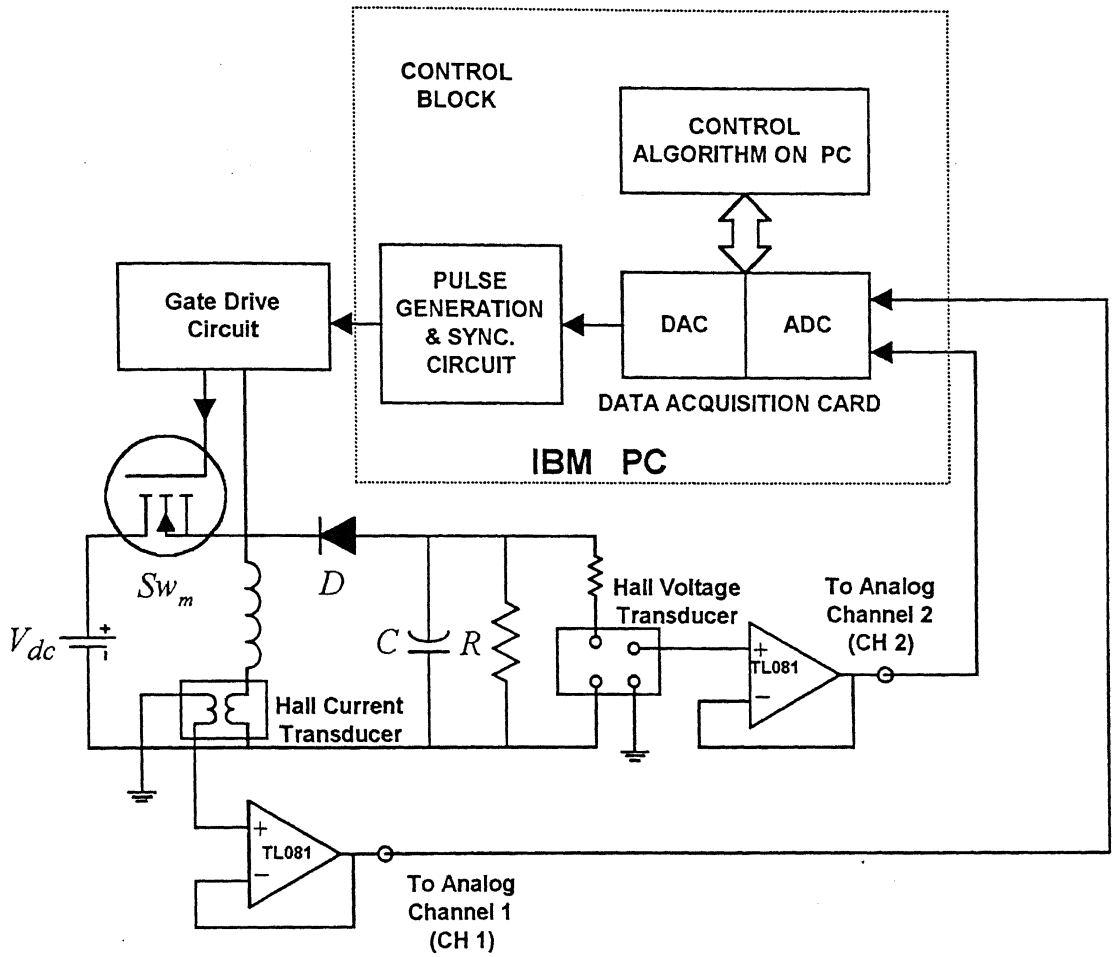


Fig. 6.4 Circuit diagram of computer controlled Buck-Boost converter.

The control block has been realized on an IBM PC along with the pulse generation and synchronization circuit as it can be seen from Fig. 6.4. The description of the control block is given in the section 6.3. Hall effect current and voltage transducers do the measurements of state variables of the converter as well as the isolation of power circuit from the control circuit. The outputs of the hall transducers are buffered by unity gain operational amplifiers. TL081 has been used for successful operation of the circuit both at low and high frequencies of the converter operation.

The inductance is designed and fabricated on a ferrite core as given in [3, 69]. The inductor is designed to have an inductance of 3 *m*H and must have a current carrying capacity of 4A without saturation. The design steps are not shown here. The

inductor has been fabricated on an EE-65 Ferrite core. There are 120 number of turns of the twisted pair of 26 SWG copper wire on the EE-65 Ferrite core. The core has air gap of 2 mm to avoid saturation of the core. The inductor has an inductance of 3mH and a quality factor of 150 at 20 kHz as measured on LCR meter. The output capacitor of the Buck-Boost is electrolytic capacitor of 330 μF. The output capacitor acts as a low pass filter and therefore electrostatic capacitor has been used. However, the ac component of the output voltage requires a high speed capacitor and therefore a 10 nF ac capacitor is also connected in parallel to the electrostatic capacitor in the output.

The number of turns in the primary coil of the Hall effect voltage and current transducers has been calculated as per the specifications given in the data sheet of these transducers to obtain a desired scaling factor. The details of the parameter determination are not given here. The details of the transducer's parameters and their scaling factors are as follows:

Current Transducer:

No. Of turns=13; Meter resistance=150Ω and scaling factor=1.875 Volts/Amperes

Voltage Transducer:

Shunt resistance=10KΩ, Meter resistance = 150 Ω, Multiplying Factor=26.668

Unity gain non-inverting amplifier as shown in above in Fig. 6.4 buffers the outputs of these transducers. The outputs of these buffers are fed to the analog to digital converter (ADC) port of the data acquisition card of the IBM computer. It is to be noted that the scaling and the multiplying factors are of the transducers only. The overall multiplying or scaling factor can be different from these values as they can be modified by voltage divider circuit and/or op-amp based multiplier circuit depending on requirements. The effective scaling factor for a set of the experiment for a particular verification is marked along with the respective experimental results.

loop experiments of the modified converter has been carried out on PC. The control block shown in Fig. 6.4 consists of a pulse generation and synchronization circuit, a data acquisition card (consisting of analog to digital converter (ADC), Digital to Analog Converter (DAC), Digital input ports) and a control algorithm in form of a computer program residing in the computer memory. Each of these blocks will be explained in following subsections.

6.3.1 PULSE GENERATION AND SYNCHRONIZATION CIRCUIT

The pulse generation and synchronization circuit is based on IC SG 3524 and its circuit diagram is given below (Fig. 6.5). The detail of this IC is given in its data sheet [68]. It has an oscillator circuit, a comparator circuit and logic circuit for producing latched output. The output stage of the IC has got a transistor pair to improve the driving capability. The oscillator circuit of SG 3524 uses external resistance R to establish a constant charging current into the external capacitor C. The charging current is equal to $3.6\,Volts/R$ and advised to keep it below $30\mu A$ to $20mA$, i.e. $1.8K < R < 100K$. The range of capacitance has also a limit as discharge time of capacitor determine the pulse width of the oscillator output pulse. The practical value of the capacitor is between 0.001 and 1.0mfd. The oscillator period is approximately $t = RC$. Where t is in μs, R in Ω and C is in μF. Besides this, there are a number of tables given to select component values. The values of R and C on pin 6 & 7are set as per the specification given in the data sheet.

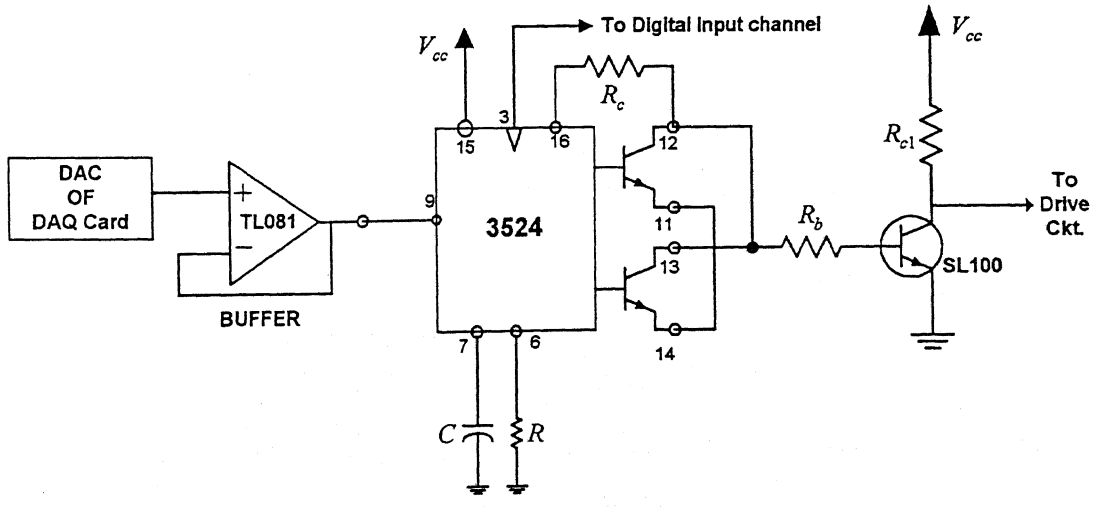


Fig. 6.5 Pulse Generation and Synchronization circuit

The details of design are straightforward and therefore are not presented here. However, The designed component values are given here.

$C = 0.022\mu F$ $R = 1.8K\Omega, R_c = R_{c1} = 1.2K\Omega, R_b = 600\Omega$ $V_{cc} = 12V$

The pin 7 of the 3524 chip produces a saw tooth waveform and it is compared with voltage applied on pin 9. Fig. 6.6 shows the generated saw tooth waveform as observed on oscilloscope. The saw-tooth waveform is synchronized with oscillator pulses available on pin 3 as can be seen from Fig. 6.6. The pulse generation circuit in this oscillogram is operating at a frequency of 54 kHz. We can see some common mode noise appearing as high frequency oscillation in ground and saw tooth signal traces.

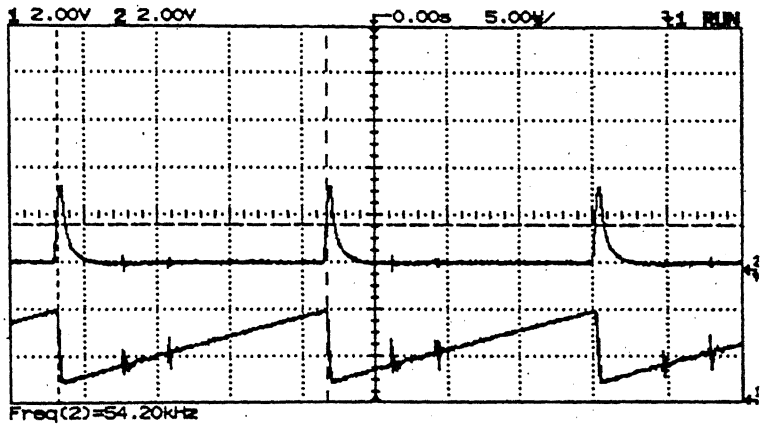


Fig.6.6 Oscillogram of the oscillator pulse of 3524 on channel 2 and triangular wave on channel 1

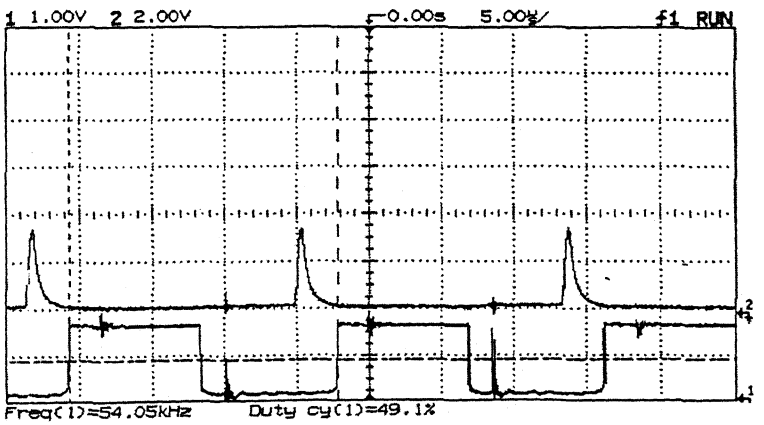


Fig.6.7 Oscillator pulse of 3524 on channel 2 on top and pulses for gate drive circuit on channel 1 at the bottom

The internal transistor pair at the output in the output stage of 3524 is connected

as shown in Fig. 6.4 to get a duty cycle in range 0 to 90% [68]. The output is connected to transistor to increase the driving capacity. The output of pulse generation circuit is shown in Fig. 6.7. Similar high frequency noise appears in the output. Note that a external transistor SL100 based buffering has been done for the output.

The output of the drive circuit is isolated replica of the gate drive pulses available from 3524 with nearly 1μsec delay. The delay is of critical significance if the converter is operating at very large duty cycle. This condition is avoided in both open loop and close loop by putting software saturation at 0.85 duty. The open loop and close loop experimentation has been done on computer.

6.3.2 Data Acquisition & PC Interface

There are two types of experiments done with the help of the computer. One is open loop experiment and another is closed loop experiment. In case of the open loop experiments, the computer acts as a simple duty ratio to control voltage converter. A desired ratio is inputted through the keyboard of the computer. There is a simple program, which converts duty ratio into control voltage. The converted control voltage through a digital to analog (DAC) port of data acquisition card is fed to the pulse generation circuit.

The data acquisition card has only two DAC ports and hence the open loop experiments for the two output-modified DC-DC converter has an additional hardware circuit along with the computer control block.

The closed loop experiments computes the duty and hence the control voltage for the pulse generation circuit from the states of the converter at the last corner point. By states of the converter, we mean inductor current and capacitor voltage in case of conventional Buck-Boost converter. The inputting of the variable at the corner point requires determination of the corner point. It can be seen from Figs. 6.6 and 6.7 that the oscillator output at pin 3 of 3524 is nearly at the corner point. This pulse has been therefore used for determination of the instant of occurrence of the corner point. Similarly this also marks the beginning of the next switching cycle and thus it also acts as synchronization pulse. This pulse is inputted through a digital input port.

The signals applied to the data acquisition card should be isolated from the

power and control circuit. Three isolated power supplies are used as shown in Fig. 6.4. One is for the power circuit, another is for the driver circuit of the power MOS switch and third is for the control block. The ground of control block is the common ground of PC and pulse and synchronization circuit. The signals from the hall transducer and oscillator of the 3524 have been brought through a 4-wire flat cable to minimize the noise. Details of the interface card are given in [74].

The ADC unit takes nearly 5μSec for conversion of analog signal into digital value and the DAC takes insignificant time. Thus, ADC is limiting factor for computer controlled system. The computation of duty by control laws given in the Chapter 3 takes nearly 1μSec on Pentium II processor at 250 MHz. The time delays are calculated off-line for obtaining the limiting value of duty ratio at a given switching frequency in the closed loop operation of the converter.

6.3.3 OPEN LOOP EXPERIMENTATION

If y_{max} & y_{min} are maximum and minimum voltage levels of the saw tooth waveform of on pin 7 of 3524, then it can be easily proved from the Fig. 6.8 that the a square wave of duty ratio d requires a control voltage of V_c volts given by equation (6.1). This control voltage is applied to pin 9 of SG 3524.

$$V_c = d\, y_{max} + (1-d)\, y_{min} \tag{6.1}$$

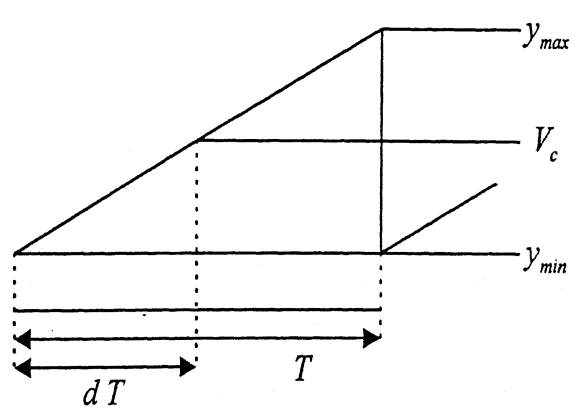


Fig. 6.8 Determination of the control voltage for Pulse Generation Circuit

The algorithm for running the converter in open circuit at a desired duty ratio is given below. This is coded in C and the executable file of the program is run on IBM

PC for calculation of the control voltage V_c. The computed value is outputted to digital to analog (DAC) port of the data acquisition card. The output of the DAC is connected to pin 9 of 3524 after buffering.

Algorithm:

begin

Set Count

Repeat

Read Duty cycle

Compute V_c from Equation (6.1).

If $V_c <= 0$

$V_c == 0$

Else if $V_c >= y_{max}$

$V_c = y_{max}$

End if

Compute equivalent binary word of V_c taking in account of scaling factor of digital to analog converter, if any

Output binary word on DAC port

Count = Count – 1

Repeat until Count = = 0

End

Some of the oscillograms of the power circuit are shown below (Fig. 6.9 to 6.11).

It can be seen from these diagrams that there exists loading of the drive circuit and noise propagation from power circuit of the converter. The output voltage shows a large content of the switching transient in the top trace of the Fig. 6.10. This may be due to improper tuning of the Snubber circuit. Similarly, the drain to source voltage shown in top trace of Fig. 6.11 shows distortions due to loading. Therefore, a further

improvement in design can be done. However the error is not severe and can serve our purpose of verification of the ideas. Due to said reasons; the experimental waveforms will not match exactly with the simulation results.

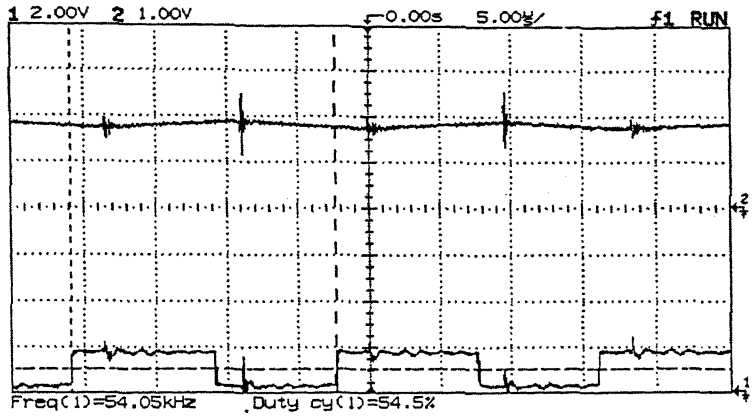


Fig.6.9 Capacitor voltage and gate drive circuit, delay is due to storage scope

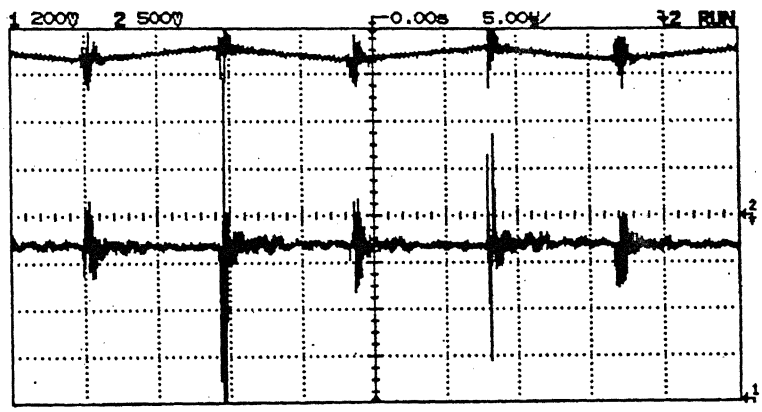


Fig.6.10 Output voltage is bottom trace, channel 1 and inductor current on channel 2.

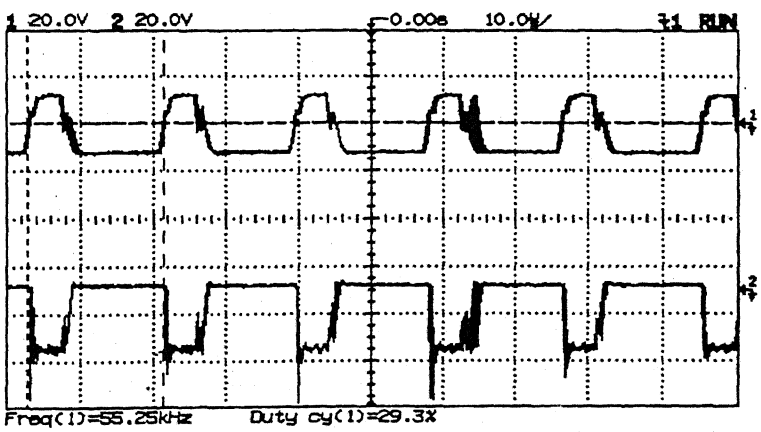


Fig. 6.11 Top trace of drain to source voltage of MOS. & bottom trace of anode to cathode voltage of diode

6.4 CONTROL ALGORITHM FOR CLOSE LOOP EXPERIMENT

The flow chart of the algorithm used for controller is given in Fig. 6.12. The digital input port of the data acquisition card is read continuously till positive to negative going edge is detected. At this instant, the switch *Sw* is switched ON. The capacitor voltage and inductor currents are samples at this instant and hold for analog to digital conversion. The inductor current is converted first and the capacitor voltage follows this. The end of conversion is sensed first before digital conversion of next data is started. This is done by reading the status bit of the ADC. Once both the states are input the control law is executed to find $\tilde{d}$. The perturbation is added to the steady state duty *d*. The computed duty is then converted in equivalent DAC data, which is outputted to DAC channel of the data acquisition card. This cycle is repeated for a number of cycles as desired. The ADC values are also stored in an array of float data, which after execution of the program is stored in a file for further processing.

6.5 MODIFIED FLYBACK CONVERTER IN OPEN LOOP

The experimental setup for verification of modified single output Buck-Boost converter studied in chapter 4 is described in this section. The circuit diagram of the modified Buck-Boost converter is shown in Fig. 4.1. The gate of the control switch (MOSFET) is shown open in Fig. 4.1. The gating pulse generation will be discussed here for the converter operating in open loop and close loop.

6.5.1 Gating Pulse Generation for Open Loop Operation of Single Output modified Buck-Boost Converter

The generation of gating pulse for open loop experimentation can be explained with help of Fig. 6.13. Let a saw tooth wave of a frequency equal to switching frequency desired of the converter is generated by some means. The saw tooth waveform thus generated is shown on the top of the Fig. 6.13. This waveform is compared by two dc values marked "A" and "B" in the figure by two comparator. The outputs of these comparator are signals marked "C" and "D". The wave with small pulse width is fed directly to main switch and switching pulse for the load switch is derived from these signals. Thus, signal "D" is fed to main switch. The truth table for gating pulse of load switch is given below in table 6.1.

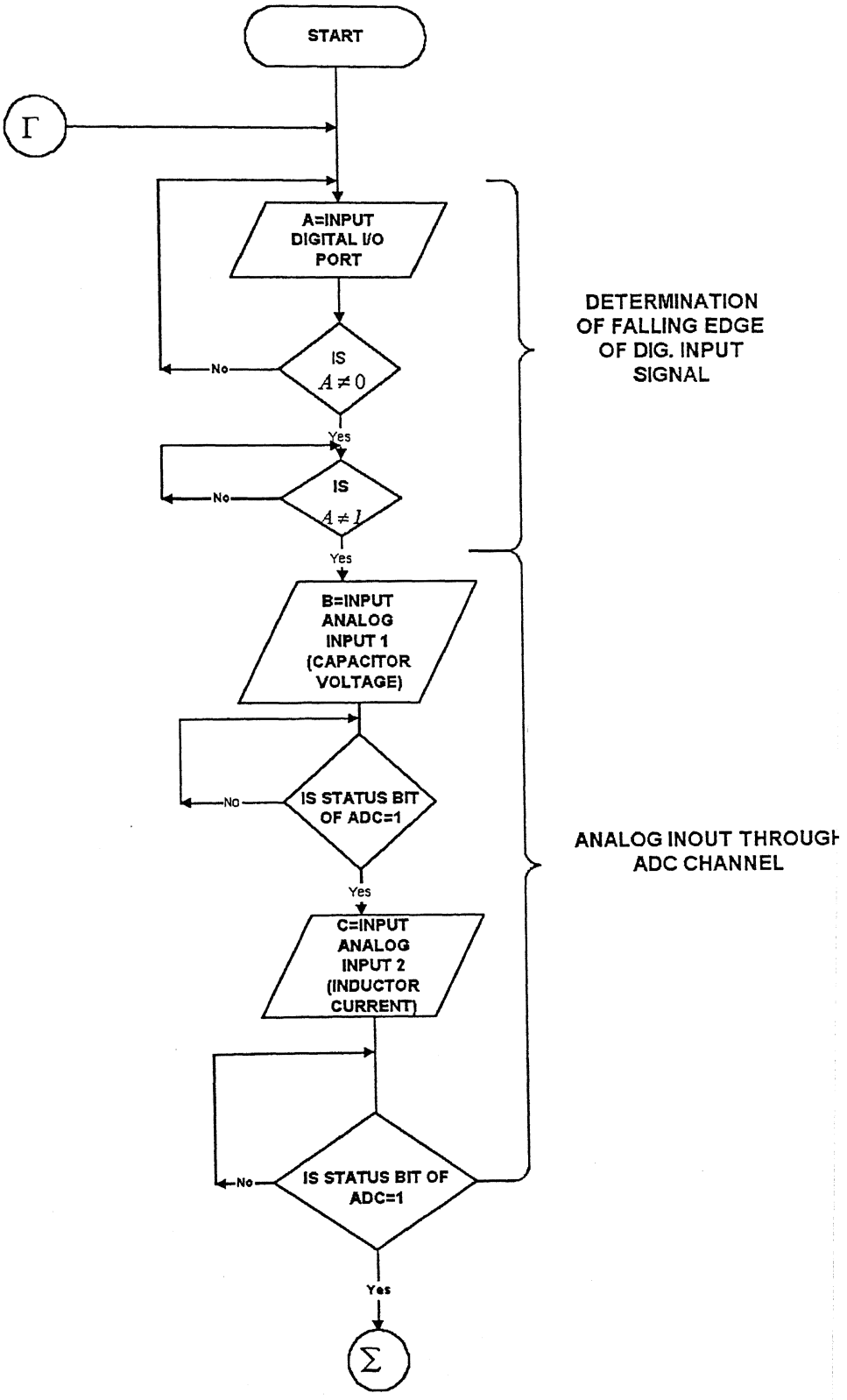


Fig. 6.12 Flow chart of the controller (Contd.)

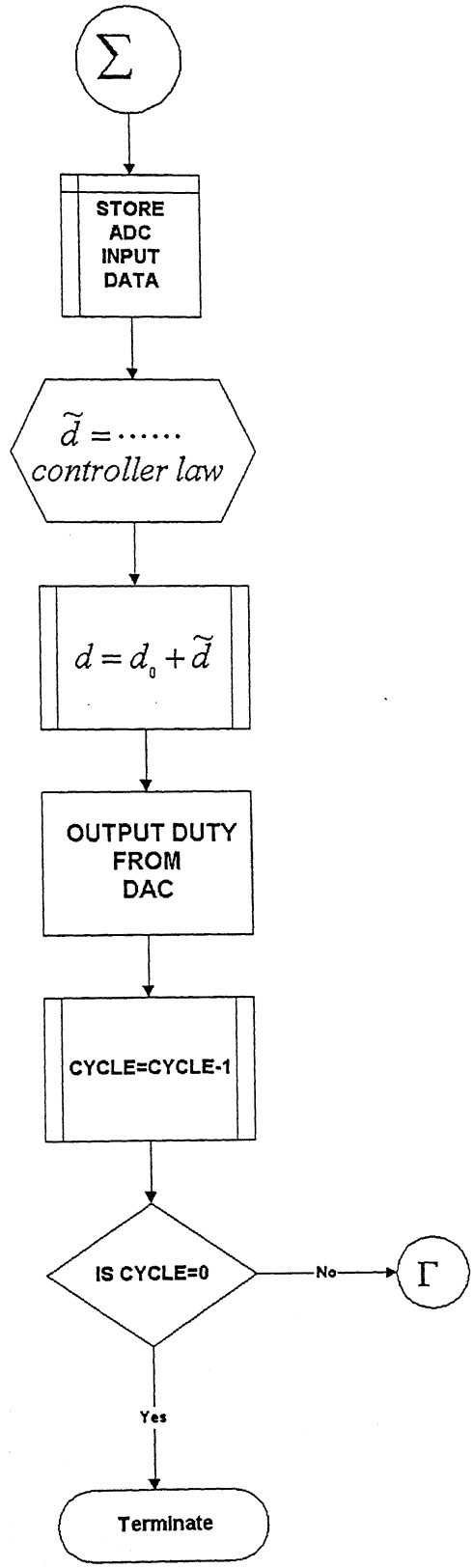


Fig. 6.12 Flow chart of the controller

Table 6.1 Gate logic

C	D	E
0	0	0
0	1	0
1	0	1
1	1	0

The truth table can be realized in a number of ways. We have taken the following realization for this.

$$E = (C \oplus D)\text{AND}(\bar{C})$$

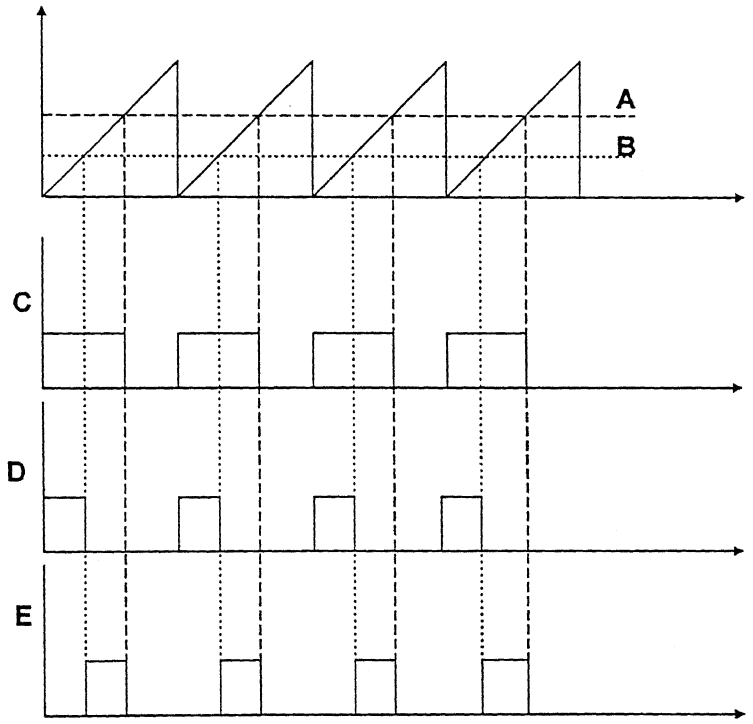


Fig. 6.13 Gate pulse generation for two switch single output modified buck-boost converter

This concept has been realized in hardware shown in Fig. 6.15. IC 3524 has been used for generating saw tooth waveform. This IC also contains a comparator. The two DAC (Digital to Analogue) channels of data acquisition card is used for getting two dc values to be fed to a comparator. The outputs of the DAC are buffered. The saw tooth waveform at pin 7 of IC 3524 is also buffered. The buffered dc value from DAC is fed to pin 9 of IC 3524, which is comparator-input point. Another input is internally

connected to saw tooth. The output of this comparator is connected in such a way that can give 90% duty cycle. The output (pin 12) of IC 3524 is fed to main switch through a common emitter transistor. This acts as buffer to the output of the IC 3524.

The buffered saw tooth is compared with another dc value on external comparator (LM 311). The output of the comparator then is logic circuit, an ex-or (7486) followed by an AND gate (7408). The out of the AND gate is buffered by common emitter transistor before connecting it to driver circuit of the load switch.

The experimental signal waveforms are shown below in Fig. 6.14. The top waveform is of saw-tooth waveform. The one below this is the waveform corresponding to signal "C" of Fig. 6.13. The waveform shown in the oscillogram next to the bottom trace is the signal corresponding to "D" and the bottom waveform of the Fig. 6.15 is equivalent to signal "E" of Fig. 6.13. We can see form the Fig. 6.14 that there are small delay associated with gating pulses, which is due to device characteristics and are unavoidable. The traces shown in Fig. 6.14 are at switching frequency of 48 kHz. There are spurious signals in some of the traces. These signals are probably due to malfunctioning of the comparator in the circuit. The circuit has noise pick up from some sources. These signals are however not going to effect the power circuits and hence not removed.

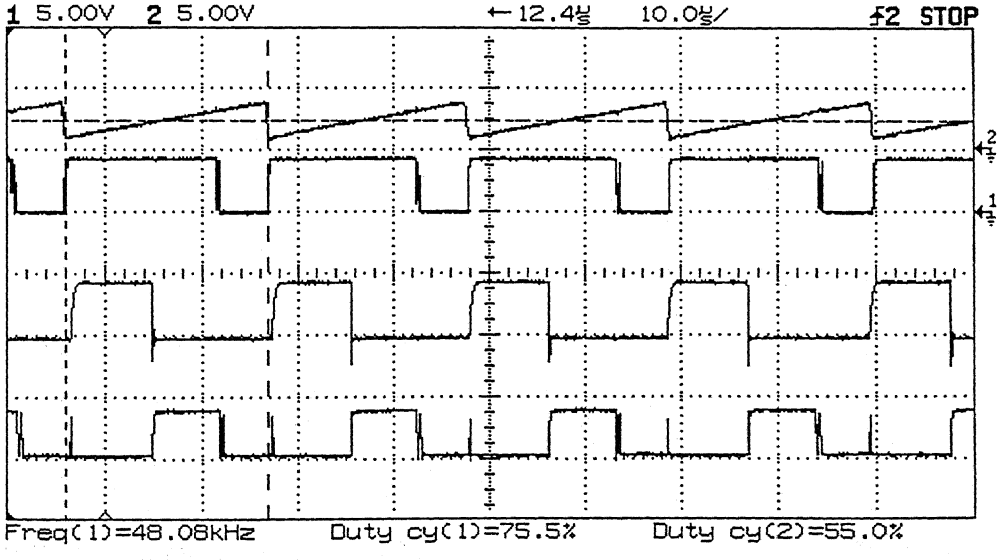


Fig. 6.14 Experimental waveforms for gate pulse generation of a modified Buck-Boost converter

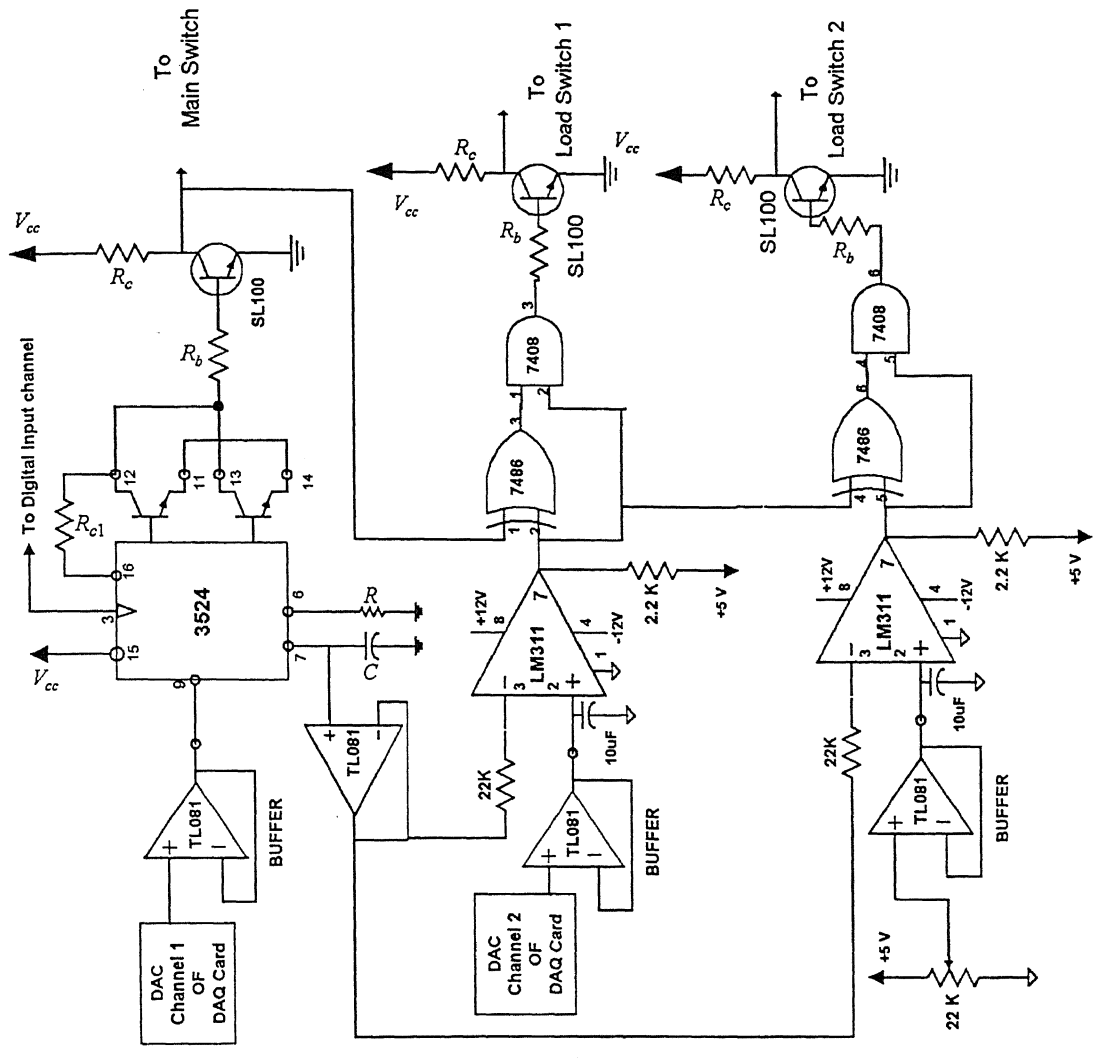


Fig.6.15 Circuit diagrams for open loop operation of single output modified flyback converter

6.5.2 Gating Pulse Generation for Open Loop Operation of Modified Two-Output Buck-Boost Converter

The principle of generation of gating pulse for multiple output converter is similar to that of the single output converter. The saw tooth waveform here is compared by three dc values rather than two. The gate pulse for main switch and load switch 1 is genrated in the same as signle output converter gate pulse. It is to be noted that the Data Acquisition Card (DAQ) has only digital to analog (DAC) ports and hence the third control voltage is generated externally. The complete open loop experimental set up for open loop experiment has been given in Fig. 6.16. A change in duty of load switch of second output require manual adjustment.

6.6 HARDWARE SETUP FOR CLOSE LOOP OPERATION OF THE MODIFIED BUCK-BOOST CONVERTER

A hysteresis close loop controller has been proposed in chapter 5 for both single output and multiple (Two) outputs modified Buck-Boost converters. In this section, the hardware realization of the hysteresis controller will be discussed. As already discussed, the hysteresis controller has two constituents, namely hysteresis voltage controller and hysteresis current controller.

Let us define the following terms to state the operation of hysteresis controller. If the variable of a circuit is to be controlled within a hysteresis band Δ around a reference ψ, then

$$\text{Lower limit} = (\psi - \Delta).$$

$$\text{Upper Limit} = (\psi + \Delta).$$

By variable, we mean core mmf or the capacitor voltage of the circuit. In case of closed loop operation of the modified converter as discussed in Chapter 5, both core mmf and output voltage is taken as references and we have two hysteresis controllers for these two variables. The principles of operation of hysteresis controllers are simple and can be stated as follows.

If Variable $\leq$ lower limit or the set point

turn ON the switch (such that the variable under consideration increases its value)

Elseif Variable $\geq$ Upper Limit

turn OFF the switch (such that the variable under consideration decreases its value)

End.

The above algorithm discusses the switching criterion for the switches. However, the gating pulses are required to be latched, i.e. if a switch is turned ON as per the algorithm stated above, it must remain in ON position till it satisfies the OFF condition and same is true in the OFF condition. Therefore, the hardware realization of the above algorithm follows by a SR latch.

The voltage and current control loop requires a window comparator, where the width

of the window is the width of the hysteresis band. The voltage and current transducers measuring the circuit parameters require scaling. The current loop is actually maintaining a constant mmf in the transformer. Therefore the current loop requires scaled adder unit which adds primary current and secondary current times the turn ratio. The adder has been realized by an inverting amplifier. It therefore requires an inverter. The set and reset condition has been derived from the comparator outputs by digital logic. This is followed by a SR (set-Reset) latch in both current and voltage loops. The circuit used in experiment has been shown in Fig. 3.17.

6.6.1 Setup For Single Output Modified Buck-Boost Converter

The gating signal arrangement for close loop operation of single output modified converter is shown in Fig. 3.18. The mmf channel or current control loop is given higher priority compared to the output voltage channel. To do this, the reset output of the controller marked $\overline{Q}_A$ of the current loop is made the enable signal for the voltage control loop. Thus, the voltage loop is only enabled when the current loop is in OFF condition.

6.6.2 Setup For Two-Output Modified Buck-Boost Converter

The block diagram of the close loop hysteresis controller for multiple (two)-output modified Buck-Boost converter is shown in Fig. 6.19. This circuit has an additional output, which requires gating of the additional load switch. The gating scheme for main switch and load switch 1 remains the same as for the single output. The priority among the load switches must be decided for gate pulse generation of the 2nd load switch. It is to be noted here that the switching of the load circuits is sequential rather than parallel. A parallel switching can be done provided we have special design for magnetic circuit. The circuit diagram shown below has highest priority to current loop, this followed by load switch 1 and finally load switch 2. The enable signal is derived from the signals at higher priority. Thus, the enable signal for load switch 1 is derived from the main switch and enable signal for load switch 2 is derived from load switch 1. The elements of the control loops are derived from Fig. 3.16.

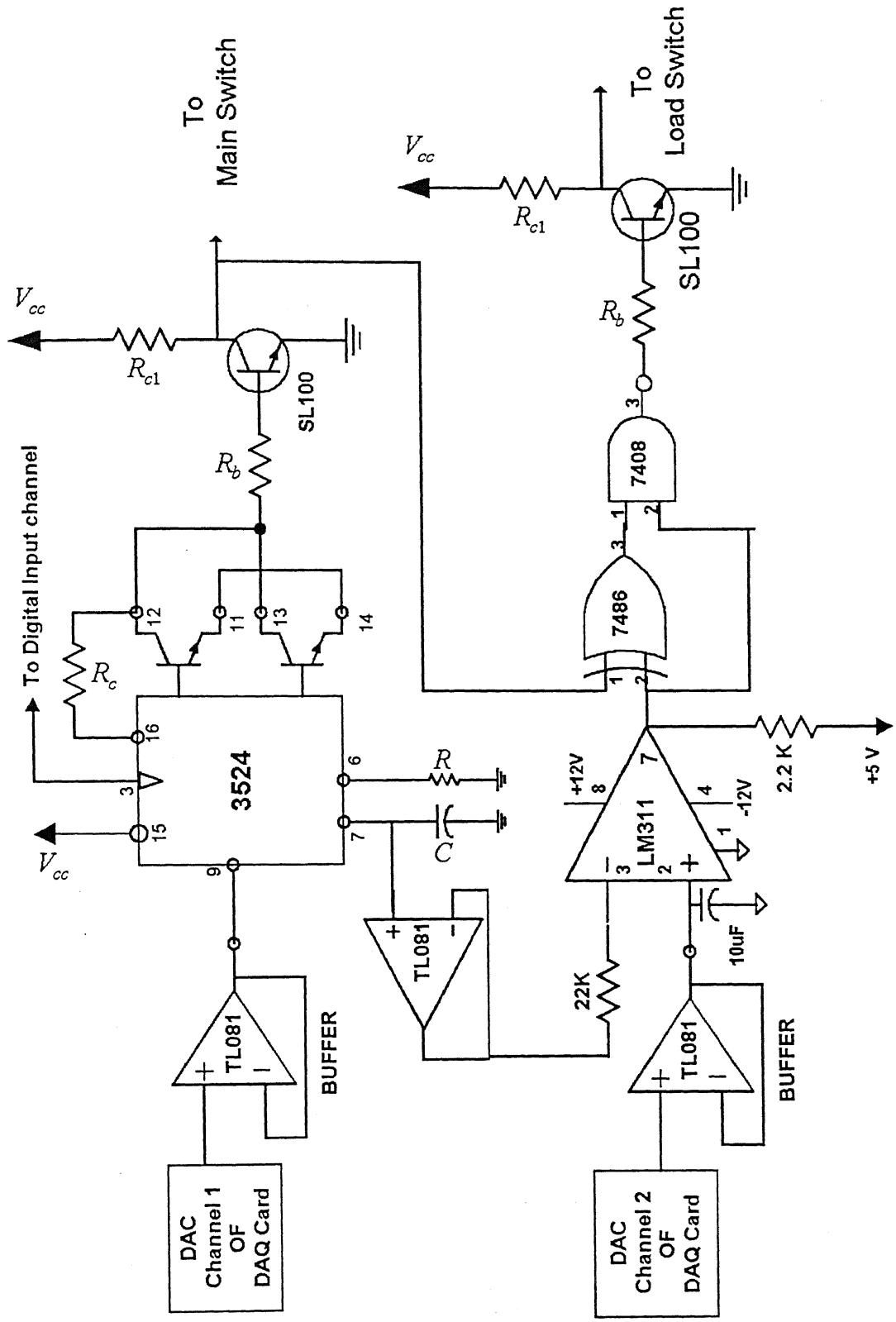


Fig.6.16 Circuit diagrams for open loop operation of Multi-output (2-output) modified flyback converter

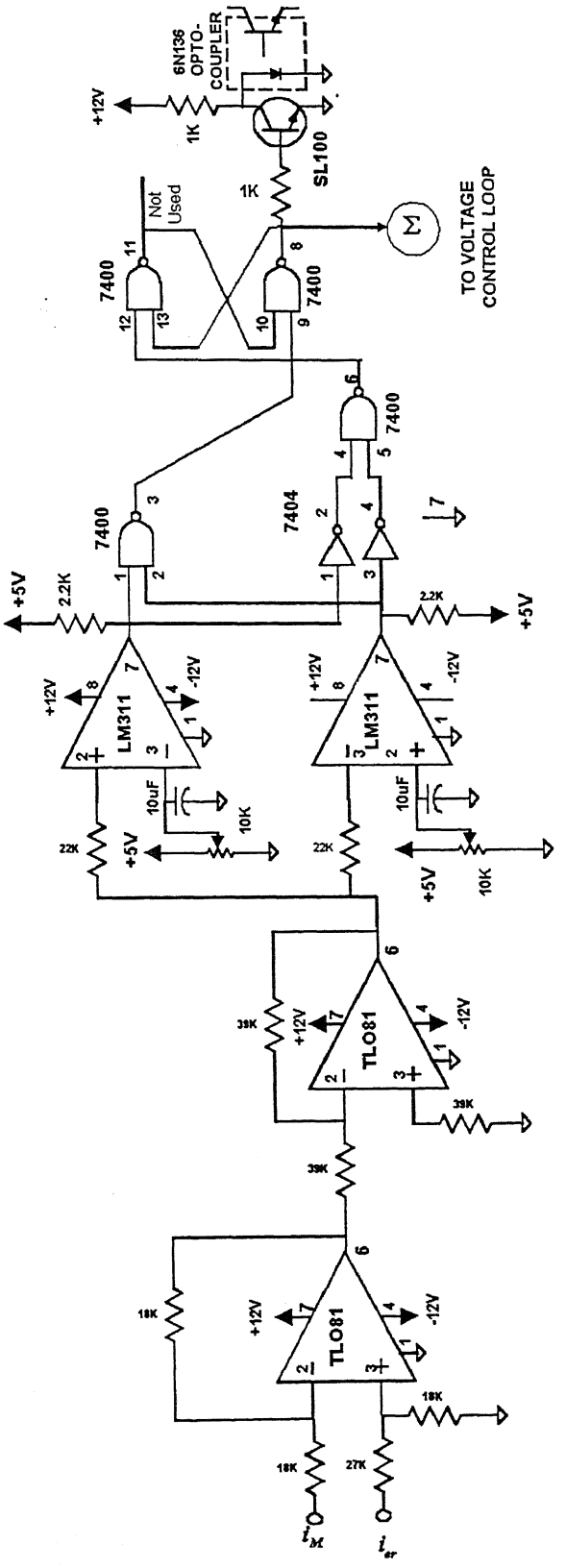


Fig.6.17 (a) Hysteresis Current control loop

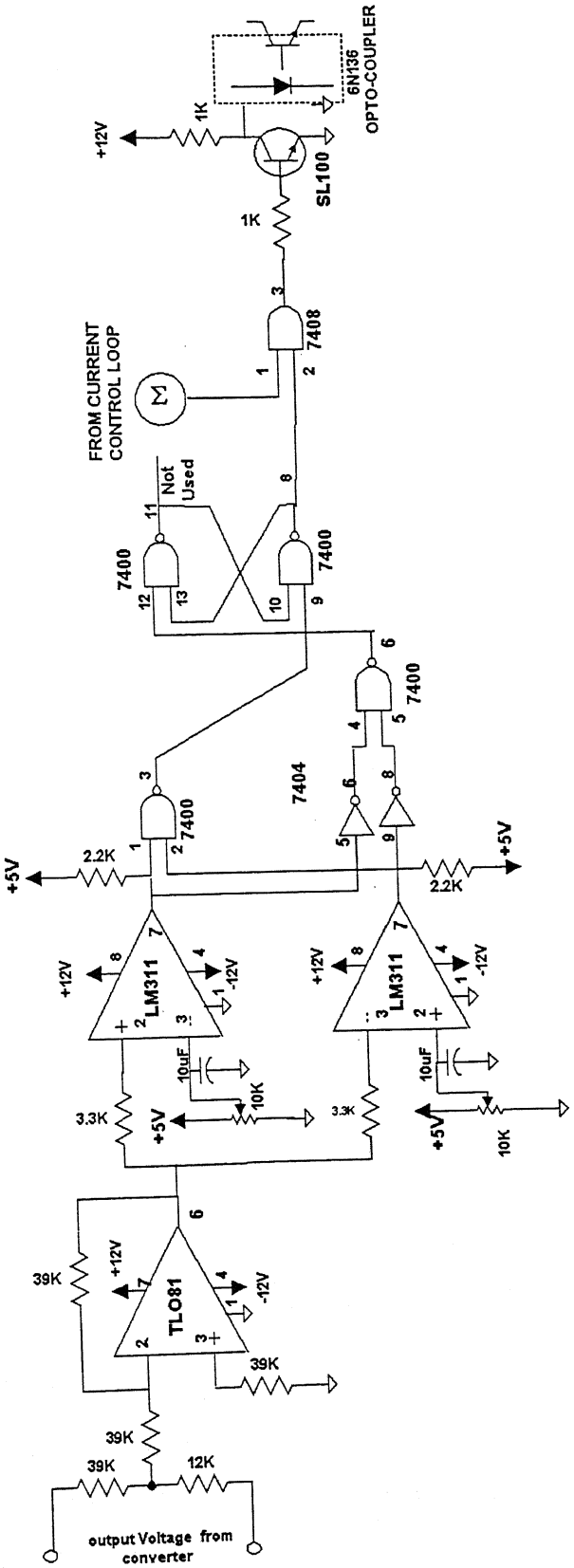


Fig.6.17 (b) Hysteresis Voltage control loop

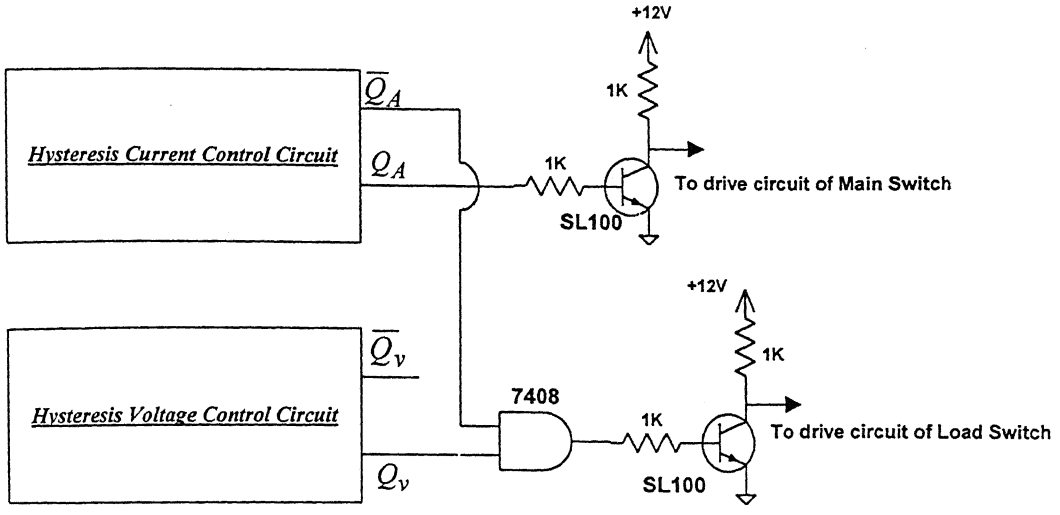


Fig. 6.18 Block diagram of hysteresis control circuit of two switch single output converter

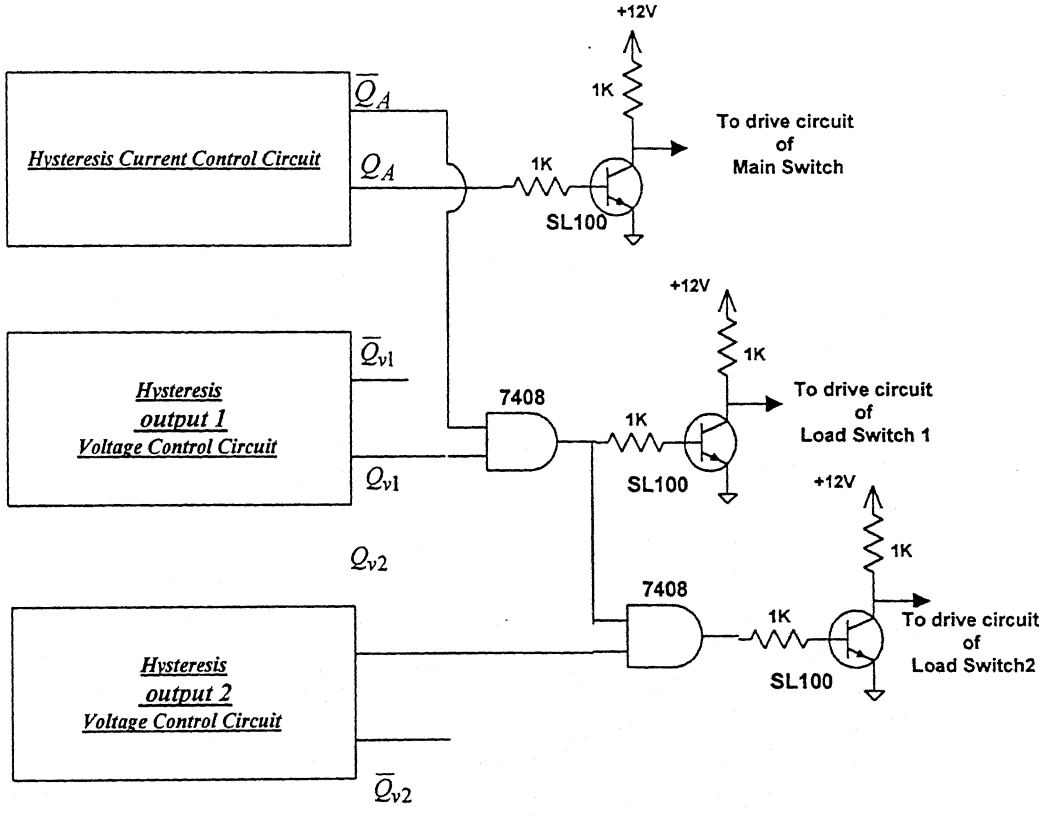


Fig. 6.19 Block diagram of hysteresis control circuit of multiple (Two) output converter

6.7 CONCLUSIONS

In this chapter the details of different circuits that are fabricated is discussed. Th photographs of the laboratory set up are shown in Fig. 6.20 through 6.22.

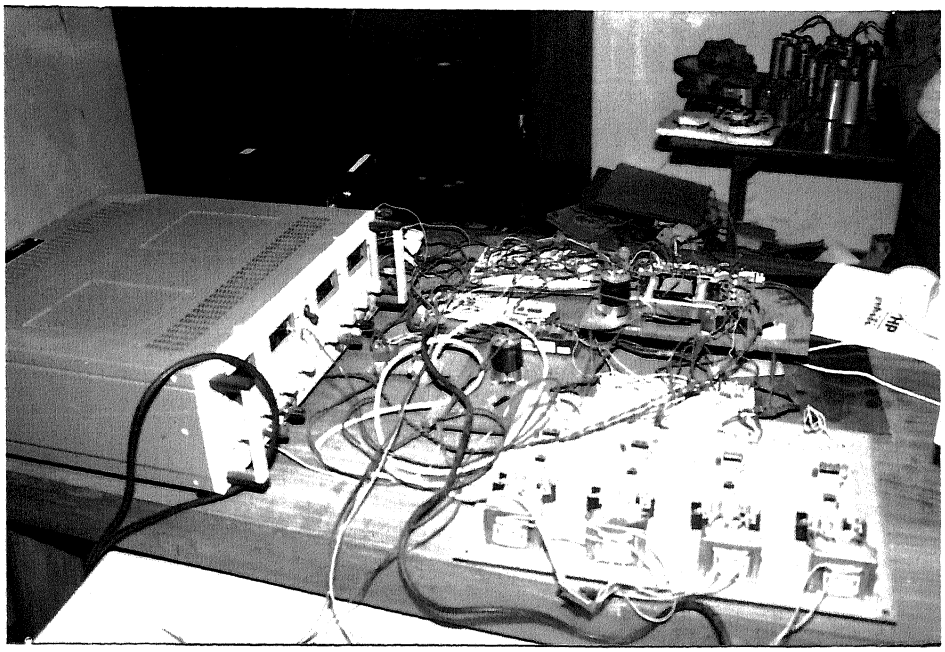


Fig. 6.20 Photograph of the experimental setup the gate drive is in Focus

Fig. 6.21 Photograph of the experimental setup the IBM PC is in Focus

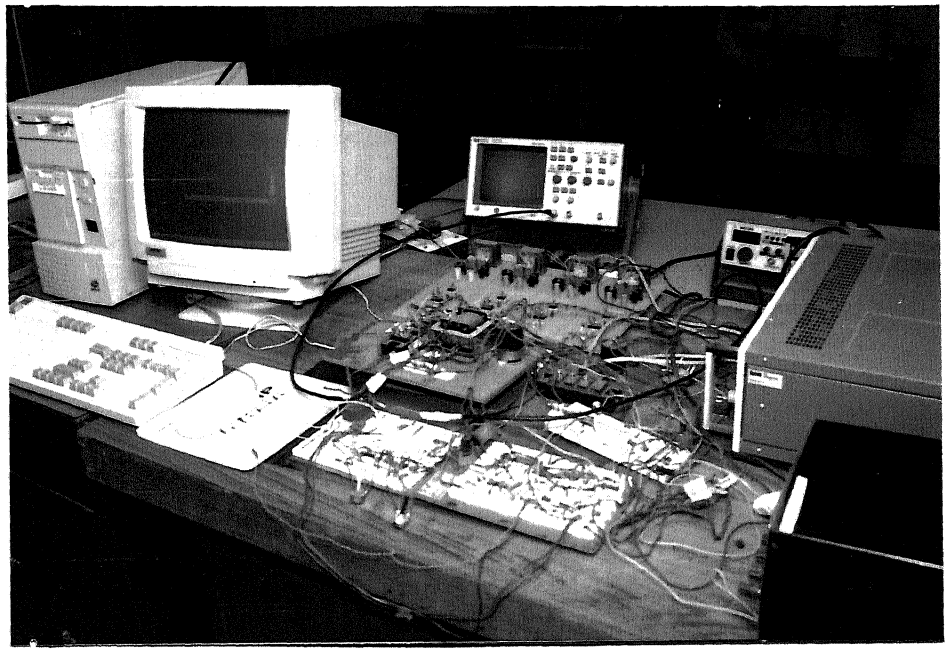


Fig. 6.21 Photograph of the complete experimental setup

CHAPTER 7

CONCLUSIONS

The general conclusions drawn from the thesis and some suggested new directions are presented in this chapter. The objective of this thesis is to design a closed loop DC-DC converter system which is capable of tracking any voltage reference with rejection of the disturbances occurring in load and supply of the converter. Further, if the conventional converter topology requires a modification for improvement in the performance the modified converter topology has to be analyzed and a suitable closed loop controller is to be designed. The closed loop converter system is expected to handle large perturbations in the tracking command and disturbances in the load and the supply. The controller must be capable of working at low frequency (≤ 10kHz) of operation as well as at higher frequency ($> 25kHz$).

7.1 GENERAL CONCLUSIONS

The work done in this thesis to achieve the above-mentioned objectives is summarized below.

7.1.1 Bilinear Corner Point and Average Modeling

Discrete time bilinear corner point prediction model of the converter in open loop has been developed and verified by extensive simulation and experimentation. The

modeling error reduces substantially compared to linear prediction model at low switching frequency and large perturbation in duty ratio.

An average bilinear model of the converter is also proposed and verified. An exact average value of the state is computed by integration of the states over a cycle. Taylor's series expansion of this average solution is truncated to obtain the bilinear model. Due to approximation made at the end, the modeling error reduces considerably. The bilinear average model thus obtained is a function of perturbation in the corner point and duty ratio. The corner point is not approximated to be equal to the average value as done in state space averaging method. The average model therefore uses the BCP model for corner point calculation. The model performs better than the state space averaging method.

7.1.2 Generalized bilinear model

Generally modeling is done for a converter which completes a switching cycle in two subintervals. A number of new topologies of the converter require more than two sub-intervals in a switching cycle. The bilinear converter model has been extended for multi-subinterval converters. The perturbation modeling of the modified buck-boost converter topology serves as an example of this concept. The model has been verified by simulation study. The proposed generalized model can therefore be applied to any converter having more than two subintervals.

7.1.3 Design of Closed loop Controller

Based on the linear and bilinear models of the converter, closed loop controller has been designed. The linear model based controller has been designed using the pole placement and the linear quadratic regulator design methods. The closed loop system has been verified by extensive simulation and experimentation. The closed loop controllers are tested for tracking step change and disturbance rejection of the load and the supply. The linear controller is capable of tracking 100% change in the reference command. The performance of linear quadratic based controller is better than the pole placement based controller.

The inductor of buck-boost converter in the experiment saturates during a part

the transient operation. The controller remains stable despite the saturation of the inductor. Therefore it can be said that the closed loop system is robust.

A closed loop controller has also been designed for the converter based on the bilinear model. Two novel methods are suggested for tracking control of the closed loop. They are named as the 'controller based on pseudo-integral action' and 'controller based on pure integral action'. The pseudo-integral based controller is computationally less extensive and has a performance similar to the pure integral based controller. Therefore, the pseudo-integral based closed loop system has been verified by both simulation study and experimentation, whereas the pure integral based system is only simulated.

The control action of the closed loop system based on the bilinear model is smoother and is capable of tracking 175 % change in the reference command, which is higher than the controller based on the linear model. The improvement in control performance is due to better modeling performance of the converter.

In order to extend the tracking capability of the closed loop system, multi-zonal fuzzy controller has been designed. The tracking range of the controller improves but the control action becomes coarse. A simulation study has been done to verify the closed loop performance.

7.1.4 Steady state analysis of modified buck-boost converter

The conventional Buck-Boost converter topology has been modified and it has beer named Modified Buck-Boost Converter. The rationale behind the modification i improvement in the dynamic response. The input-output relationship of the modifie converter has been derived. The converter is capable of operating in the buck and the boos modes of operation.

The modified converter topology has been extended for multiple outputs. The inpu output relationship of the converter in steady state at constant frequency has been derive The outputs at constant frequency have cross-regulation between outputs. It therefo requires a variable frequency operation to utilize the potential of the converter.

Small signal modeling of the modified buck-boost converter has been done using the generalized bilinear model. The small signal model is bilinear in the main and the load duty ratios. Due to this, the perturbation model of single output modified converter becomes mathematically too complex. It will therefore require a highly complicated closed loop control design. Further, this will be computationally too extensive and hence closed loop controller is not designed for constant frequency operation.

7.1.5 Hysteresis controller

As said earlier, the small signal of modified converter is mathematically complex and hence some alternate closed loop controller is required. A hysteresis controller has been designed to operate in the close loop. It operates at variable frequency during transients. Extensive simulation study and experiment have verified the hysteresis-controlled closed loop controller for the modified converter. The closed loop hysteresis controller has a fast dynamics and capable of tracking larger tracking voltage compared to the closed loop controller of buck-boost converter.

7.1.6 Hardware Implementation

PC interface is used for implementation of the proposed controllers based on linear and bilinear models. The use of PC makes the system more flexible for conducting experiments. This has helped us to test the complicated control laws.

7.2 SCOPE FOR FUTURE WORK

Some of the suggested new directions of the research in the area of modeling and control design for dc-dc converter are as foolows

1. Modeling of the converter may be extended for DCM mode of operation of the converter.

2. The Fuzzy controller may be developed further to obtain smoother control action.

3. The modified converter topology can be analyzed in variable frequency mode and a small signal model may be derived.

4. The hysteresis controller can be mathematically modeled in closed loop to get the zone of stable operation.

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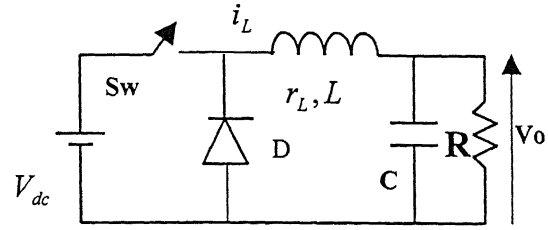
APPENDIX-A

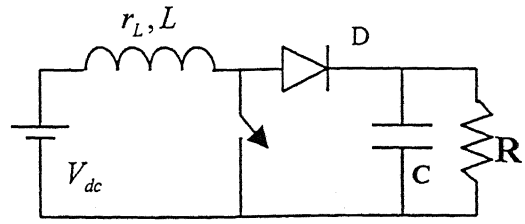
CONVERTER CIRCUITS, PARAMETERS & MODEL

A.1 CONVERTER CIRCUITS AND PARAMETERS

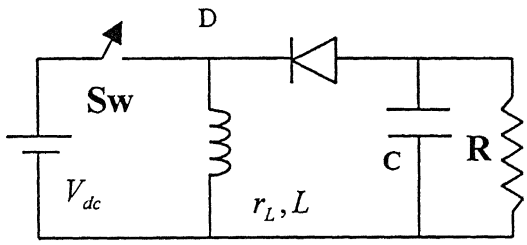
The circuit diagrams of various converters are given below.



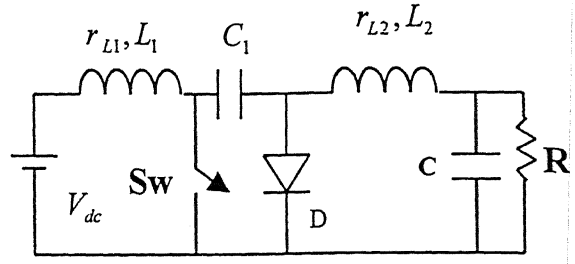
(a) Buck Converter



(b) Boost Converter



(c) Buck - Boost



(d) Cuk Converter

The dynamic equations for these converters are given below.

Buck Converter: The switch ON equations are given by

$$V_{dc} + r_L i_L + L\frac{di_L}{dt} + v_0 = 0 \quad \text{and} \quad i_L = C\frac{dv_0}{dt} + \frac{v_0}{R} \qquad 0 < t < dT \qquad \text{(A.1}$$

Where r_L is the internal resistance of the choke inductor. The voltage and current equation for the circuit when switch is OFF and the diode is conducting is given by,

$$r_L i_L + L\frac{di_L}{dt} + v_0 = 0 \qquad \text{and } i_L = C\frac{dv_0}{dt} + \frac{v_0}{R} \qquad dT < t < T \qquad \text{(A.2)}$$

Let the state vector be $x = [v_o \quad i_L]^T$ and let the A_1, A_2, B_1 and B_2 are state and inpu matrices for switch on and off respectively. These matrices are obtained by solving the above mentioned equations. We get the following

$$A_1 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & -r_L/L \end{bmatrix} \; ; \; B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix} \text{ and } A_2 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & -r_L/L \end{bmatrix} \; ; \; B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad \text{(A.3)}$$

Boost Converter: The circuit diagram of a boost converter is given in Fig. (b). Le us assume the circuit operates in CCM. . The A_1, A_2, B_1 and B_2 are derived from th differential equations of the state variables in switch ON and OFF positions as done in th buck converter discussed above, assuming the elements to be ideal.

The voltage and current equation for switch ON are given by

$$V_{dc} = r_L i_L + L\frac{di_L}{dt} \qquad \text{And } C\frac{dv_0}{dt} + \frac{v_0}{R} = 0 \qquad 0 < t < dT \qquad \text{(A.4}$$

The voltage and current equations for the circuit when switch is OFF and the diode conducting is given by,

$$r_L i_L + L\frac{di_L}{dt} + v_0 = V_{dc} \qquad \text{And} \qquad i_L = C\frac{dv_0}{dt} + \frac{v_0}{R} \qquad dT < t < T \qquad \text{(A.}$$

$$A_1 = \begin{bmatrix} -1/RC & 0 \\ 0 & -r_L/L \end{bmatrix} \qquad A_2 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & -r_L/L \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix} \qquad B_2 = B_1 \qquad \text{(A.}$$

Buck-Boost Converter: The differential equations of the converter states are

$$V_{dc} = r_L i_L + L\frac{di_L}{dt} \qquad C\frac{dv_0}{dt} + \frac{v_0}{R} = 0 \qquad 0 < t < dT \tag{A.7}$$

$$r_L i_L + L\frac{di_L}{dt} + v_0 = 0 \qquad \text{And } i_L = C\frac{dv_0}{dt} + \frac{v_0}{R} \qquad dT < t < T \tag{A.8}$$

Which in state space form is given by

$$A_1 = \begin{bmatrix} -1/RC & 0 \\ 0 & -r_L/L \end{bmatrix} \qquad A_2 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & -r_L/L \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix} \qquad B_2 = \mathbf{0} \tag{A.9}$$

Cŭk Converter: The circuit diagram of this converter has been shown in Fig (d) above.

$$V_{dc} = r_{L1} i_{L1} + L_1 \frac{di_{L1}}{dt} \qquad 0 < t < dT$$

$$V_{dc} = r_L i + L_1 \frac{di_{L1}}{dt} + v_0 \qquad dT < t < T$$

$$i_{L2} = C\frac{dv_0}{dt} + \frac{v_0}{R} \qquad 0 < t < T$$

$$v_{C1} = r_{L2} i_{L2} + L_2 \frac{di_{L2}}{dt} + v_0 \qquad 0 < t < dT \tag{A.10}$$

$$0 = r_{L2} i_{L2} + L_2 \frac{di_{L2}}{dt} + v_0 \qquad dT < t < T$$

$$C\frac{dv_{C1}}{dt} = -i_{L2} \qquad 0 < t < dT$$

$$C\frac{dv_{C1}}{dt} = i_{L1} \qquad dT < t < T$$

From the above written differential equation of the states, we derive here the state space equations. Let the state vector be given by $x = [v_0 \quad v_{C1} \quad i_{L1} \quad i_{L2}]$.

$$A_1 = \begin{bmatrix} -1/CR & 0 & 0 & 1/C \\ 0 & 0 & 0 & 1/C_1 \\ 0 & 0 & -r_{L1}/L_1 & 0 \\ -1/L_2 & 1/L_2 & 0 & -r_{L2}/L_2 \end{bmatrix} \qquad B_1 = \begin{bmatrix} 0 \\ 0 \\ 1/L_1 \\ 0 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -1/CR & 0 & 0 & 1/C \\ 0 & 0 & 1/C & 0 \\ -1/L_1 & 0 & -r_{L1}/L_1 & 0 \\ -1/L_2 & 0 & 0 & -r_{L2}/L_2 \end{bmatrix} \qquad B_2 = B_1 \qquad \text{(A.11)}$$

Modified Buck-Boost converter Converter: The differential equations of the converter states are

$$V_{dc} = (r_{L1} + r_{sw} + r_{in})\frac{\Im}{N_1} + \frac{L_1}{N_1}\frac{d\Im}{dt} \qquad C(R + r_c)\frac{dv_c}{dt} = -v_0 \qquad 0 < t < DT_S$$

$$r_L\frac{\Im}{N_1} + \frac{L_1}{N_1}\frac{d\Im}{dt} + v_c + Cr_c\frac{dv_c}{dt} = 0 \text{ and } \frac{\Im}{N_1} = C\frac{dv_0}{dt} + \left(v_c + Cr_c\frac{dv_c}{dt}\right)\frac{1}{R} \qquad DT_S < t < d\ T_S$$

$$-V_{dc} = (r_{L2} + r_d + r_{in})\frac{\Im}{N_2} + \frac{L_2}{N_2}\frac{d\Im}{dt} \qquad C(R + r_c)\frac{dv_c}{dt} = -v_0 \quad dT_S < t < T_S \qquad \text{(A.12)}$$

Where r_{L1} and r_{L2} are the resistance of the primary winding and secondary resistance of respectively of the energy recovery winding and r_{sw}, r_d & r_{in} are switch, diode and source

resistance respectively. The core mmf is taken as one the state variable and it has been represented in above equations by $\Im$.

Let $r_L = r_{L1} + r_{sw} + r_{in}$ and $\rho = r_{L2} + r_d + r_{in}$.

$$A_1 = \begin{bmatrix} -1/(R+r_c)C & 0 \\ 0 & -r_L/L_1 \end{bmatrix} \qquad B_1 = \begin{bmatrix} 0 \\ N_1/L_1 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -1/(R+r_c)C & R/(R+r_c)N_1C \\ -\frac{N_1}{L_1}\left(1-\frac{r_c}{R+r_c}\right) & (-)\left\{\frac{r_{L1}}{L_1}+\frac{r_c}{L_1(R+r_c)}\right\} \end{bmatrix} \qquad B_2 = \mathbf{0}$$

$$A_3 = \begin{bmatrix} -1/(R+r_c)C & 0 \\ 0 & -\rho/L_2 \end{bmatrix} \qquad B_3 = \begin{bmatrix} 0 \\ -N_2/L_2 \end{bmatrix} \qquad \text{(A.13)}$$

In case of DCM operation of the converter, it enters into a fourth phase. During thi interval, the converter has only capacitor discharging goes on. If the state matrices ar represented by A_4 and B_4, these are given by

$$A_4 = \begin{bmatrix} -1/(R+r_c)C & 0 \\ 0 & 0 \end{bmatrix} \qquad B_4 = \mathbf{0}. \qquad \text{(A.14}$$

PARAMETERS

The parameters of Buck-Boost have been taken from the reference [Ghosh] and this maintained same for Buck and Boost Converters. The resistance of the inductor is assum very small typical value.

$L = 4.0\ mH$, $r_L = 1.2\Omega$ $\quad C = 25\mu F$ $\quad R = 10\Omega$ $\quad V_{dc} = 100V$

$L = 3.0\ mH$, $C = 300\mu F$, $R = 5\Omega$. $V_{dc} = 20V$, $f = 1500\ Hz$ Natural Frequency=1054 I

The parameters of cŭk converter are taken from example taken in [kugi99].

$L_1 = 50mH \quad r_{L1} = 0.86 \quad L_2 = 10mH \quad r_{L2} = 1.18\Omega \quad C = 100\mu F \quad C_1 = 680\mu F$

$R = 10\Omega$

A.2 Derivation of Linear Perturbation Model

$$x(t_2) = \Phi_2\Phi_1 x(t_0) + (\Phi_2\Theta_1 + \Theta_2)V_{dc} \tag{A1.1}$$

where Φ_1, Φ_2, Θ_1 and Θ_2 are the matrices evaluated at d_0. The Taylor's series expansio of (A1.1) yields

$$\tilde{x}(t_2) = \Phi_2\Phi_1\big|_{d_0}\tilde{x}(t_0) + \frac{\partial}{\partial d}\left(\Phi_2\Phi_1 x(t_0) + \Phi_2\Theta_1 + \Theta_2)V_{dc}\right)$$

$$= \Phi_2\Phi_1\big|_{d_0}\tilde{x}(t_0) + \left[\frac{\partial\Phi_2}{\partial d}\Phi_1 x(t_0) + \Phi_2\frac{\partial\Phi_1}{\partial d}x(t_0) + \frac{\partial\Phi_2}{\partial d}\Theta_1 V_{dc} + \Phi_2\frac{\partial\Theta_1}{\partial d}V_{dc} + \frac{\partial\Theta_2}{\partial d}V_{dc}\right]\tilde{d}$$

(A1.2

Now from equations (2.7) and (2.10), we get

$$\frac{\partial\Phi_1}{\partial d} = A_1\Phi_1 T\ \big|_{d_0} \ \&\ \frac{\partial\Phi_2}{\partial d} = -A_2\Phi_2 T\ \big|_{d_0}$$

Again note that if A_1 is nonsingular then we get from equation (2.8)

$$\Theta_1 = \left[A_1^{-1}\left(e^{A_1 dT} - I\right)\right]B_1$$

Thus,

$$\frac{\partial}{\partial d}\Theta_1 = \left[A_1^{-1}A_1 e^{A_1 dT}\right]B_1 T = \Phi_1 B_1 T\ \big|_{d_0}$$

Similarly, if A_2 is nonsingular then we get from equation (2.11)

$$\Theta_2 = \left[A_2^{-1}\left(e^{A_2(1-d)T} - I\right)\right]B_2$$

and hence $$\frac{\partial}{\partial d}\Theta_2 = -\left[A_2^{-1}A_2 e^{A_2(1-d)T}\right]B_2 T = -\Phi_2 B_2 T \Big|_{d_0}$$

Thus substituting in (A1.2) we get

$$\tilde{x}(t_2) = F\tilde{x}(t_0) + G\tilde{d}(t_0) \qquad \text{(A1.3)}$$

Where $$F = \Phi_2\Phi_1$$

$$G = (\Phi_2 A_1 \Phi_1 T_c - A_2\Phi_2\Phi_1 T_c) * X(t_0) + (\Phi_2 B_1 T_c - A_2\Phi_2 B_1 T_c^2 d_0) * V_d$$

In the above formulation we have assumed that the matrices are nonsingular. This howeve may always not be true. For example, the matrix A_1 for buck-boost converter is given i equation (2.1) is singular. In this case we have to find $\frac{d\Theta_1}{d(d)}$ using a different approach. Fo this the state transition matrix is given by

$$\Phi_1 = e^{A_1 dT} = \begin{bmatrix} e^{-t/RC} & 0 \\ 0 & 1 \end{bmatrix}$$

then
$$\Theta_1 = \int_0^{dT} \begin{bmatrix} e^{-(dT-\eta)/RC} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1/L \end{bmatrix} d\eta$$
$$= \int_0^{dT} B_1 d\eta = B_1 dT$$

Hence $$\frac{\partial\Theta_1}{\partial d} = B_1 dT$$

However, since $\Phi_1 B_1 = B_1$, we can write $$\frac{\partial\Theta_1}{\partial d} = \Phi_1 B_1 dT$$

which is the same as obtained before.

A.3 Integration used in Average Model

The integration of x (t) has got two components. The one is the integral of the stat transition matrix with respect to time and the other involves integral of θ with respect t time. Let us first simplify these integrals for a general case and this will then be substitute in the equation (2.20) to find the average. Let us take first the integral of the state transitio matrix

$$\int_0^{dT} e^{A_1 t}\,dt = A_1^{-1} e^{A_1 t}\Big|_0^{dT} = A_1^{-1}(\Phi_1 - I)$$

Similarly, $$\int_0^{(1-d)T} e^{A_2 t}\,dt = A_2^{-1} e^{A_2 t}\Big|_0^{(1-d)T_c} = A_2^{-1}(\Phi_2 - I)$$

The integral of Θ_1 with respect to t is shown below.

$$\int_o^{dT} \Theta_1(t)dt = \int_{dT0}^{dT} \int e^{A_1 t} B_1 V_d\,dt = \int_0^{dT} A_1^{-1}\left[e^{A_1 t} - I\right] B_1 V_d\,dt$$
$$= \int_0^{} dT B_1 V_d\,dt = d^2 T^2 B_1 V_d$$

Similarly, $$\int_0^{(1-d)T} \Theta_2(t)dt = (1-d)^2 T^2 B_2 V_d$$

By the Taylor's series expansion of (2.25), the coefficients for the perturbation model for buck-boost converter are obtained and are given by the following equation.

$$F_{av} = d * I + (1-d) * \Phi_1 + A_1 (dT)^2 / 2T + \Phi_1 A_2 (1-d)^2 T/2$$

$$G_{av} = (I - \Phi_1 - A_2 \Phi_1 (1-d)T + A_1 dT + A_1 \Phi_1 (1-d) * T) * x(t_0) + (1-d) * \Phi_1 B_1 V_d T$$

$$H_{av} = I - \Phi_1 (I + A_2 * (1-d) * T) + A_2 dT$$

APPENDIX-B

BILINEAR CONTROL DESIGN

As mentioned in section 3.2 that a Lyapunov function candidate of the form

$$V(k) = \tilde{x}_e^T(k) P \tilde{x}_e(k) \tag{B.1}$$

is chosen and the control is designed to ensure that $\Delta V(k) = V(k+1) - V(k)$ is negative definite. Note that we can rewrite (B.1) as

$$V(k+1) = \tilde{x}_e^T(k+1) P \tilde{x}_e(k+1) \tag{B.2}$$

such that

$$\Delta V(k) = \tilde{x}_e^T(k+1) P \tilde{x}_e(k+1) - \tilde{x}_e^T(k) P \tilde{x}_e(k) \le 0 \tag{B.3}$$

B.1 Controller with Pseudo- Integrator

Substituting the extended state equation (3.11) in (B.3) and rearranging we get

$$\Delta V(k) = \tilde{x}_e^T(k) \left[F_e^T P F_e - P \right] \tilde{x}_e + \Im(\tilde{x}_e, \tilde{u}) \tag{B.4}$$

where

$$\begin{aligned} \Im &= \tilde{x}_e^T(k) F_e^T P\, G_e \tilde{u}(k) + \tilde{x}_e^T(k) F_e^T P\, H_e \tilde{x}_e(k) \tilde{u}(k) + \tilde{x}_e^T(k) F_e^T P\, J_e \tilde{y}_{ref} \\ &+ \left[G_e^T + \tilde{x}_e^T(k) H_e^T \right] \tilde{u}(k)\, P\, F_e \tilde{x}_e(k) + \left[G_e^T + \tilde{x}_e^T(k) H_e^T \right] P \left[G_e + H_e \tilde{x}_e(k) \right] \tilde{u}^2(k) \\ &+ \left[G_e^T + \tilde{x}_e^T(k) H_e^T \right] P\, J_e \tilde{y}_{ref}(k) \tilde{u}(k) + J_e^T \tilde{y}_{ref}(k)\, P\, F_e \tilde{x}_e(k) \\ &+ J_e^T \tilde{y}_{ref}(k)\, P \left(G_e + H_e \tilde{x}_e(k) \right) \tilde{u}(k) + J_e^T \tilde{y}_{ref}(k)\, P\, J_e \tilde{y}_{ref} \end{aligned} \tag{B.5}$$

For a given matrix F_e and a arbitrarily chosen positive definite matrix Q, we can find positive definite matrix P, such that $\left[F_e^T P F_e - P \right] = -Q$. This makes first term on RHS the equation a negative definite matrix. The remaining term is minimized with respect control input $\tilde{u}(k)$. Minimization of this term makes the RHS to be negative defini thereby ensuring the stability of the closed loop system. For minimization, we require

$$\frac{d\Im}{d\tilde{u}} = 0 \tag{B.}$$

Solving (B.5) and (B.6) for the $\tilde{u}(k)$, we get

$$\tilde{u}(k) = \frac{-\tilde{x}_e^T(k)F_e^T P(G_e + H_e\tilde{x}_e(k)) - \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]PJ_e(k)\tilde{y}_{ref}(k)}{G_e^T PG_e + \tilde{x}_e^T(k)H_e^T\left[2G_e + H_e\tilde{x}_e(k)\right]} \quad \text{(B.7)}$$

B.2 Controller with Pure Integrator

Substituting the extended state equation (3.18) in (B.3) and rearranging we get

$$\Delta V(k) =$$
$$\left[F_e\tilde{x}_e(k) + G_e v(k) + H_e\tilde{x}_e(k)v(k) - H_1\tilde{x}_e(k)L\tilde{x}_e(k) + J_1\tilde{y}_{ref}(k)\right]^T P$$
$$\left[F_e\tilde{x}_e(k) + G_e v(k) + H_e\tilde{x}_e(k)v(k) - H_1\tilde{x}_e(k)L\tilde{x}_e(k) + J_1\tilde{y}_{ref}(k)\right] - \tilde{x}_e^T P\tilde{x}_e$$
$$\Delta V(k) = \tilde{x}_e^T(k)\left[F_e^T PF_e - P\right]\tilde{x}_e + \Im(\tilde{x}_e, v, k) \quad \text{(B.8)}$$

Where

$$\Im = \tilde{x}_e^T(k)F_e^T P\, G_e v(k) + \tilde{x}_e^T(k)F_e^T P\, H_e\tilde{x}_e(k)v(k) + \tilde{x}_e^T(k)F_e^T P\left[J_e\tilde{y}_{ref} - H_1\tilde{x}_e(k)L\tilde{x}_e(k\right.$$
$$+ \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]v(k)\, P\, F_e\tilde{x}_e(k) + \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[G_e + H_e\tilde{x}_e(k)\right]v^2(k)$$
$$+ \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[J_e\tilde{y}_{ref}(k) - H_1\tilde{x}_e(k)\, L\tilde{x}_e(k)\right]v(k)$$
$$+ \left[J_e^T\tilde{y}_{ref}(k) - \tilde{x}_e^T(k)L^T\tilde{x}_e^T(k)H_1^T\right]P\, F_e\tilde{x}_e(k)$$
$$+ \left[J_e^T\tilde{y}_{ref}(k) - \tilde{x}_e^T(k)L^T\tilde{x}_e^T(k)H_1^T\right]P\left(G_e + H_e\tilde{x}_e(k)\right)v(k)$$
$$+ \left[J_e^T\tilde{y}_{ref}(k) - \tilde{x}_e^T(k)L^T\tilde{x}_e^T(k)H_1^T\right]P\left[J_e\tilde{y}_{ref} - H_1\tilde{x}_e(k)L\tilde{x}_e(k)\right]$$

The control action is obtained by minimization of the function $\Im$ as done above

$$\frac{d\Im}{dv} = 0$$

$$0 = \tilde{x}_e^T(k)F_e^T PG_e + \tilde{x}_e^T(k)F_e^T PH_e\tilde{x}_e(k) + 0$$
$$+ \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]PF_e\tilde{x}_e(k) + 2*\left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[G_e + H_e\tilde{x}_e(k)\right]v(k)$$
$$+ \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[J_e\tilde{y}_{ref}(k) - H_1\tilde{x}_e(k)L\tilde{x}_e(k)\right]$$
$$+ 0$$
$$+ \left[J_e^T\tilde{y}_{ref}(k) - \tilde{x}_e^T(k)L^T\tilde{x}_e^T(k)H_1^T\right]P\left(G_e + H_e\tilde{x}_e(k)\right)$$
$$+ 0$$

$$2*\tilde{x}_e^T(k)F_e^T PG_e + 2*\tilde{x}_e^T(k)F_e^T PH_e\tilde{x}_e(k) + 2*\left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[G_e + H_e\tilde{x}_e(k)\right]v(k)$$
$$+ 2\left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[J_e\tilde{y}_{ref}(k) - H_1\tilde{x}_e(k)L\tilde{x}_e(k)\right] = 0$$

Let $w(k) = \left[J_e\tilde{y}_{ref}(k) - H_1\tilde{x}_e(k)L\tilde{x}_e(k)\right]$

$$2*\tilde{x}_e^T(k)F_e^T PG_e + 2*\tilde{x}_e^T(k)F_e^T PH_e\tilde{x}_e(k) + 2*\left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[G_e + H_e\tilde{x}_e(k)\right]v(k)$$
$$+ 2\left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]Pw(k) = 0$$

or,

$$v(k) = \frac{-\tilde{x}_e^T(k)F_e^T P\left(G_e + H_e\tilde{x}_e(k)\right) - \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]Pw(k)}{\left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]P\left[G_e + H_e\tilde{x}_e(k)\right]} \tag{B.9}$$

or,

$$v(k) = \frac{-\tilde{x}_e^T(k)F_e^T P\left(G_e + H_e\tilde{x}_e(k)\right) - \left[G_e^T + \tilde{x}_e^T(k)H_e^T\right]Pw(k)}{G_e^T PG_e + \tilde{x}_e^T(k)H_e^T\left[2G_e + H_e\tilde{x}_e(k)\right]} \tag{B.10}$$

This is the bilinear Control law for the converter based on the Lyapunov formulation.